KU LEUVEN

ARENBERG DOCTORAL SCHOOL
Faculty of Engineering Science

Study of the Selector Element for Resistive Memory

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Dissertation presented in partial fulfillment of the requirements for the degree of Doctor in Engineering Science:
Electrical Engineering

October 2015

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Dissertation presented in partial fulfillment of the requirements for the degree of Doctor in Engineering Science: Electrical Engineering

In collaboration with:

October 2015

Acknowledgements

Writing this part of the thesis means that my Ph.D. journey finally comes to an end. Taking this opportunity, I would like to thank all the people, for being with me through the past six years. Because of you, the days in Leuven became my best memories!

Firstly of all, I would like to express my gratefulness to my promoter Prof. Guido Groeseneken and co-promoter Prof. Dirk J. Wouters. We know each other for a long time, when I was enrolled in the master program of nanoscience and nanotechnology since 2009. Thanks for selecting me as a master student that initiated my life in Belgium, and thanks for your trust that gave me the opportunity to start this exciting Ph.D. research at imec. The Ph.D. meetings with you always reviewed my progress, clearly defined the future works and timelines. Step by step, I always kept the right direction towards the destination of this Ph.D. journey. Without your continuous guidance, support, coordination and encouragement, my Ph.D. would not be carried out that smoothly!

Dr. Bogdan Govoreanu (imec), my daily supervisor, needs particular thanks for always trusting in me, being supportive of my work by providing me with all possible resources he could offer. No matter how busy his schedule was, he always squeezed his time and was ready for my questions, arranged regular meetings with me to follow my daily work, corrected my papers and presentation slides, shared his expertise and novel ideas on both technical and non-technical things. I feel so lucky that I have a supervisor like him!

Special thanks also to my Ph.D. examination committee members: Prof. Francky Catthoor (imec/KULeuven), Prof. Wim Dehaene (KULeuven), Prof. Pierre Fazan (Micron technology/EPFL) and Prof. Rainer Waser (RWTH Aachen University). Thanks for their endorsement on my Ph.D. work and giving me their valuable feedback on the manuscript to improve the quality of this dissertation!

I would like to express my gratitude to the RRAM program director at imec: Dr. Malgorzata Jurczak. She is such a kind boss who is always generous for her praise and encouragement to the Ph.D. students in the group. Next to it, I would like to

thank the following RRAM team members: Dr. Ludovic Goux, Dr. Andrea Fantini, Augusto Redolfi, Dr. Robin Degraeve, Michael Chen, Attilio Belmonte, Umberto Celano, Avasarala Naga Sruti, Georgi Gorine, Steven Folkersma. Especially the SRC team members: Davide Crotti, Dr. Christoph Adelmann, Dr. Sergiu Clima, Dr. Karl Opsomer, Dr. Mihaele Popovici, Subhali Subhechha, Dr. Alin Velea. I learned a lot from you and I feel proud of being a member of this top-class research team in the RRAM community! Moreover, I would give extra thanks to my group members/friends: Attilio, Andrea and Michael, for the wonderful conference trip memories we shared together. Indeed, the leadership from the memory department at imec: Dr. Furnemont Arnaud, Dr. Jan van Houdt, Laith Altimime deserve my special thanks, for their continuous support over the years.

There are two persons: Dr. Stefan Cosemans and Dr. Yangyin Chen, who I should give my thanks in particular. Things are always difficult at the beginning, so as my Ph.D. study. Their kind help made me to grasp the essential skills and knowledge, which stand the basis for my following research work.

Big thanks also to my imec colleagues, ex-colleagues and industrial assignees: Paul Hendrickx, Dr. Pieter Blomme, Dr. Iuliana Radu, Nico Jossart, Marc van Dievel, Joris van Laer, Tom Daenen, Albert Vanhelmont, Dr. Ben Kaczer, Dr. Eddy Simon, Dr. Jacopo Franco, Dr. Adrian Chasin, Woojin Kim, Dr. Kar Gouri Sankar, Ajay Bhoolokam, Dr. Arturo Sibaja-Hernandez, Julien Mailfert, Dr. Sven Cornelissen, Capogreco Elena, Gabriele Congedo, Dr. An Chen (Global Foundries), Dr. Kun Hou (Sandisk), Dr. Gottwald Matthias (Qualcomm), Dr. Nak Seong (ASML), Dr. Yasuhara Ryutaro (Panasonic), Dr. Zhiqiang Wei (Panasonic), Numata Toshinori (Toshiba), Masanori Komura (Toshiba), Dr. Seonggeon Park (Samsung), Dr. Kwangmin Park (Samsung), Dr. Wooyoung Park (SK Hynix), Alessio Spessot (Micron), Dr. Qi Xie (ASM), Dr. Chunmeng Dou (University of Cambridge), Dr. Liang Zhao (Crossbar), Zizhen Jiang (Standford University).

My friends and Chinese fellows, thanks for sharing your time with me in Leuven: Jie Hu, Irene Kwee, Dr. Yangyin Chen, Dr. Lianggong Wen, Dr. Yi Li, Dr. Yan Li, Qixian Shi, Chen Wu, Weiming Qiu, Menglei Xu, Dr. Shuzhen You, Ruping Cao, Ziyang Liu, Tian-Li Wu, Michael Chen, Kuang-Wei Cheng, Dr. Tung Huei Ke, Yiming Yang, Dr. Chang Chen, Dr. Bo Wang, Sijia Jiang, Hao Yu, Dr. Min Zhao, Yang-Shun Fan, Zheng Chai, Yue Pan, Dr. Daisy Zhou, Xubin Chen, Dr. Meng Li, Chunshu Li, Zheng Xu, Yanxiang Huang, Shengping Mao, Jia Shi, Dr. Weimin Gao, Dr. Kaidong Xu, Dr. Weiming Guo, Dr. Xiaopin Shi, Dr. Hu Liang, Dr. Mingxu Liu, Dr. Yunlong Li, Dr. Lei Zhang, Xuanwu Kang, Dr. Wei Guo, Dr. Riqing Zhang, Dr. Libing Zhou, Dr. Yan Cai, Dr. Chun-Hsien Huang, Xinfang Liu, Enlong Liu, Hongtao Chen, Mark Hsu, Yuandong Li, Jingdong Yan, Haodong Zhang, Shun Zhao, Yanan Hu, Shuyang Liu, Dr. Fangzhou Ling, Shuo Wang, Dr. Chun Gong, Yu Li, Dr. Wan-Yu Lin, Dr. Frank Kao, Dr. Peter Tseng, Dr. Baojun Tang, Dr. Fengying Qiao, Dr. Cheng Mei, Dr. Wen Fang, Dr. Jing Wang, Sa Xiao, Qian Xia, Xiaodan Lin and Pengfei Liang.

Apart from that, I would like to thank Prof. Yanling Shi from East China Normal University, who motivated me and recommended KULeuven and imec.

My deepest thanks belong to my family members. My grandparents-Shouxiang Zhang and Zhongwei Pan; my parents-Xiaodong Zhang and Wen Xiong, for bringing me up and their unconditional love. My uncle, Tong Gan, gave me lots of supports on my arrival in Leuven and introduced his friends to me so that I did not feel lonely in this new environment, I should thank him. My parents-in-law, Shuxing Ding and Minhua Ding, thanks for taking care of my wife during the days when I cannot return back to China to be with her. My wife, Yunying Ding, deserves my greatest appreciation. With the separation of two places which are thousands of miles apart, you made huge sacrifices to support my studies. Without your love, trust and understanding, I am not able to accomplish this work!

Leqi Zhang

October 2015

Leuven, Belgium

Abstract

This Ph.D. study focuses on the selector element for the one-selector one-resistor (1S1R) based cross-point array type resistive random access memory (RRAM). The performance requirements for implementing the selector device are derived from a circuit perspective, by employing a hybrid circuit simulation and an analytical analysis approach.

We evaluated two types of selector devices, namely the type-I selectors that generates non-linear I-V characteristics without an abrupt I-V transition, and the type-II selectors where the device is characterized by an abrupt increase of the current at a certain (threshold) voltage. We found that trade-offs exists for fulfilling the combined requirements for low voltage operation, large on/off resistance window and highly non-linear 1S1R cell characteristics. To balance these trade-offs, the operating voltage range for the type-I selectors and the threshold voltage for the type-II selectors need to be carefully designed, allowing a good voltage compatibility with the resistive memory element. Compared to the type-I selectors, the advantage of using type-II selectors is that they are more favorable for low voltage operation, while the limited design margin due to possible disturb of the memory status of the resistive memory element remains a challenge.

Furthermore, we extracted specific selector design parameters for an array with reference size of 1Mbit. Using these extracted selector parameters as a guidance, different recent selector concepts were evaluated. The promising Metal-Silicon-Metal (MSM) selector was chosen for an in-depth experimental study for understanding its performance, reliability and design trade-offs. By including thermal annealing and barrier engineering, we optimized the MSM structure resulting in an improved half-bias non-linearity of over 6000, and a high drive current over 1MA/cm^2, while the operating voltage range is compatible with a typical HfO_x-based resistive memory.

On the basis of the reference MSM selectors, a variability-aware array performance assessment is carried out. It was found that the selector is an important contributor to array variability, causing array-level read margin degradation. Thus, improved cell

characteristics are required to accommodate cell variability and ensure acceptable read performance.

Finally, the vertical 3D RRAM (VRRAM) array was analyzed. We determined the critical leakage paths in VRRAM architecture and proposed an optimized bias scheme to balance the array performance trade-offs. In addition, a comparison was made between stacked 3D cross-point arrays and VRRAM under both read and write operations.

Keywords: resistive random access memory (RRAM), selector, 1S1R, cross-point array, Metal-Silicon-Metal, variability, 3D RRAM, vertical RRAM (VRRAM).

Beknopte samenvatting

Dit doctoraatsonderzoek concentreert zich op het selector element voor de één-selector één-resistor (1S1R) cross-point array type resistive random access memory (RRAM). De performantie vereisten voor het implementeren van deze selector zijn afgeleid vanuit een circuit perspectief, door het gebruik van een hybriede circuit-simulatie en analytische analyse.

Twee types selector elementen werden geevalueerd, namelijk type-I selectoren met niet-lineaire I-V karakteristieken zonder een abrupte I-V overgang, en type-II selectoren waar het element gekarakteriseerd wordt door een abrupte toename van de stroom bij een bepaalde (drempel) spanning. Er wordt aangetoond dat compromissen nodig zijn om te voldoen aan de gecombineerde vereisten van lage spanningswerking, grote aan/uit weerstandsratio en sterk niet-lineaire 1S1R cel karakteristieken. Om deze compromissen te balanceren, moet het werkzame spanningsbereik voor type-I selectoren en de drempelspanning voor type II-selectoren zorgvuldig vastgelegd worden, om zo een goede spanningscompatibiliteit met het resistieve geheugenelement mogelijk te maken. In vergelijking met de type-I schakelaars, is het het gebruik van type-II schakelaars gunstiger is voor lage spanningswerking. De beperkte ontwerpmarge wegens mogelijke verstoring van de geheugehtoestand van het resistieve geheugenelement in de cel blijft echter een uitdaging.

Verder leidden we specifieke selector ontwerpparameters af voor een array met referentie grootte van 1 Mbit. Met deze selector ontwerpparameters als richtlijn, werden verschillende recente selectorconcepten geëvalueerd. De veelbelovende Metaal-Silicon-Metaal (MSM) selector werd uitgekozen voor een gedetailleerde experimentele studie van zijn performantie en betrouwbaarheid. Door gerbuik van thermische behandeling en barriere engineering optimaliseerden we MSM structuren met een verbeterde half-bias niet-lineariteit van meer dan 6000, en met en hoge stroomdichtheid van meer dan 1MA/cm^2, waarbij het werkzame spanningsbereik compatibel is met een typisch HfO_x-gebaseerd resistief geheugen.

Op basis van de referentie MSM selector, werd een variabiliteit includerende array

analyse uitgevoerd. Deze toonde aan dat de selector een belangrijke bijdrage geeft aan de array variabiliteit, welke leidt tot array-level degradatie van de leesmarge. Verbeterde celkenmerken zijn nodig om de celvariabiliteit op te vangen en te zorgen voor aanvaardbare leesprestaties.

Tenslotte werd de vertikale 3D RRAM (VRRAM) geanalyseerd. De kritische lekpaden in de VRRAM architectuur werden bepaald en een geoptimaliseerd bias schema werd voorgesteld om de verschillende array performantie compromissen te balanceren. Ook werd een vergelijking gemaakt van gestapelde 3D kruispunt arrays en VRRAM voor zowel lees- als schrijfoperaties.

Sleutelwoorden: resistive random access memory (RRAM), selector, 1S1R, cross-point array, Metal-Silicon-Metal, amorphous silicon, variability, 3D RRAM, vertical RRAM (VRRAM).

Abbreviations

Acronym	Description
1S1R	One-Selector One-Resistor
1T1C	One-Transistor One-Capacitor
1T1R	One-Transistor One-Resistor
AA	Activation Annealing
a-Si	Amorphous Silicon
BD	Breakdown
BE	Bottom Electrode
BEC	Bottom Electrode Contact
BiCS	Bit Cost Scalable
BL	Bit Line
BL_{ns}	Unselected Bit Line
BL_s	Selected Bit Line
BLHS	Bit-Line Half Selected
CBRAM	Conductive Bridge Random Access Memory
CC	Current Compliance
CCS	Constant Current Stress
CMO	Conductive Metal Oxide
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical-Mechanical Planarization
CRS	Complementary Resistive Switching
CTF	Charge Trap Flash
CTL	Critical Time Loop
DIBL	Drain Induced Barrier Lowering
DPT	Double patterning technology
DRAM	Dynamic Random Access Memory
DT	Direct Tunneling
E^2ROM	Electrically Erasable Programmable Read Only Memory
EELS	Electron Energy Loss Spectroscopy
EM	Electro-Migration

Acronym	Description
EPROM	Erasable Programmable Read Only memory
F	Feature size
FAST	Field Assisted Superlinear Threshold
FeRAM	Ferroelectric Random Access Memory
FN	Fowler-Nordheim
FOM	Figure-of-Merit
GST	GeSbTe
HE	Horizontal Electrode
HiZ	High Impedence
HRS	High Resistance State
IR	The voltage drop over the resistor
I-V	Current-Voltage
LPCVD	Low Pressure Chemical Vapor Deposition
LRS	Low Resistance state
M/S	Metal-Silicon Interface
MIEC	Mixed-Ionic-Electron Conduction
MIM	Metal-Insulator-Metal
MIMIM	Metal-Insulator-Metal-Insulator-Metal
MIT	Metal Insulator Transition
MLC	Multi-Level Cell
MRAM	Magnetic Random Access Memory
M-SCM	Memory-type Storage Class Memory
MSM	Metal-Silicon-Metal
NAND	Not AND digital logic
NDR	Negative Differential Resistance
NL	Non-Linearity
NOR	Not OR digital logic
NS	Non-Selected
NVM	Non-Volatile Memory
OTS	Ovonic Threshold Switching
P/E	Program and Erase
PCRAM	Phase Change Random Access Memory
PDA	Post-Deposition Anneal
PF	Poole-Frenkel
PPA	Post-Passivation Anneal
PVD	Physical Vapor Deposition
RAM	Random Access memory
RM	Read Margin
ROM	Read Only Memory
RRAM	Resistive Random Access Memory
RSE	Resistive Switching Element

Acronym	Description
RSM	Response Surface Model
RW	Resistance Window
SCM	Storage Class Memory
SEL	Selected Cell
SEM	Scanning Electron Microscopy
SILC	Stress Induced Leakage Current
SLC	Single-Level Cell
SLT	Super-Linear Threshold
SRAM	Static Random Access Memory
SRC	Self-Rectifying Cell
S-SCM	Storage-type Storage Class Memory
TAT	Trap-Assisted Tunneling
TCAD	Technology Computer Aided Design
TDDB	Time Dependent Dielectric Breakdown
TE	Top Electrode
TEC	Top Electrode Contact
TEM	Transmission Electron Microscopy
TFT	Thermal-Field Tunneling
TMO	Transition Metal Oxide
TO	Tunneling Oxide
TS	Threshold Switching
TU	TUnneling
TVS	Threshold Vacuum Switching
UTO	Ultra-Thin-HfO_x
VE	Vertical Electrode
VMCO	Vacancy Modulate Conductive Oxide
VNAND	Vertical-NAND
VRRAM	Vertical Resistive Random Access Memory
WL	Word Line
WL_{ns}	Unselected Word Line
WL_s	Selected Word Line
WLHS	Word-line Half Selected
WM	Write Margin

List of Symbols

Symbol	Unit	Description
ϕ_m	V	Metal workfunction
ϕ_{ms}	V	Metal-semiconductor workfunction difference
ψ_{bi}	V	Built-in potential
σ_r	-	Standard Deviation
E_a	eV	Activation Energy
E_{BD}	V/cm	Breakdown Field
E_c	eV	Conduction Band Energy
I_{BL}	A	Bit Line Read Current
I_{drive}	A	Drive Current
I_{hold}	A	Holding Current
$I_{readout}$	A	Readout Current
I_{ref}	A	Reference Current
$I_{switching}$	A	Switching Current
J_{max}	A	Maximum Drive Current Density
kT	eV	Boltzmann constant
$NL_{1/2}$	-	Half-bias Non-Linearity
N_d	cm^{-3}	Doping concentration
P_R	W	Read Power Consumption
P_W	W	Write Power Consumption
Q_{inj}	A/cm^2	Injected charge fluence
$q\phi_b$	eV	Barrier Height
$q\chi$	eV	Electron Affinity
RM	%	Read Margin
R_S	Ω	(On-state) Series Resistance
V_{access}	V	Access Voltage
V_{BD}	V	Breakdown Voltage
V_{dd}	V	Supplied (Write) voltage
$V_{disturb}$	V	Disturb Voltage
V_{hold}/V_H	V	Holding Voltage

Symbol	Unit	Description
V_{op}	V	Operation Voltage
V_{ox}	-	Oxygen Vacancy
V_{read}	V	Read Voltage
V_{RESET}	V	RESET Voltage
V_{sense}	V	Sensing Voltage
V_{SET}	V	SET voltage
V_{th}	V	Threshold Voltage
WM	%	Write Margin

Contents

Chapter 1

Introduction

1.1 Background

Semiconductor memory technologies play an important role in today's information society. Nowadays, semiconductor solid state memories can be found in ubiquitous electronic systems in a wide field of applications, such as computers, portable electronics, automotive applications, data centers, etc. With the rapidly increasing demand of high performance, large capacity and low cost products in the storage memory market, driven by the explosive growth of portable electronics, semiconductor non-volatile memory (NVM) market, currently dominated by Flash memory [1], has been growing very fast in recent years. Especially the NAND Flash [2], given its compact string-architecture array configuration, offers superior area efficiency, which provides the lowest cost per bit compared to other commercial NVM technologies at present, e.g. NOR Flash [3], E^2PROM [4], etc. The great success of NAND Flash comes from the aggressive scaling down of the memory cell size leading to a continuous cost reduction. However, this would come to an end in the foreseeable future, as the planar Flash memory device is expected to face its economical and physical limitations after 2015 (e.g. beyond sub-16nm technology node). On the one hand, fabrication of planar NAND Flash memory strings in a 1x nm technology node requires an extremely difficult patterning process [5], rendering the effect to excessively cut down the cost per bit by scaling to be counterproductive. On the other hand, both the reliability such as data retention and program endurance, and the cell-to-cell uniformity become much worse, due to a low amount of stored charges for the scaled devices. This is why recently, a non-planar 3D vertical structure was proposed for NAND Flash, known as "BiCS" (Bit-Cost Scalable) technology [6]. In this 3D configuration, NAND cell strings are formed in the vertical direction. Bit per cost scaling, therefore, can be driven

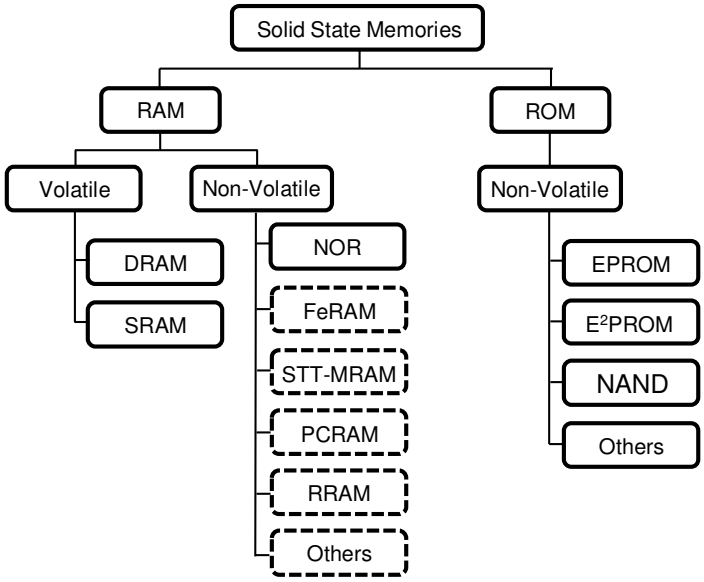


Figure 1.1: *Classification of semiconductor solid state memories. The emerging memory technologies, e.g. FeRAM, STT-MRAM, PCRAM, RRAM are circled in dash-box.*

by stacking additional memory layers, instead of pursuing aggressive lateral scaling, which would seriously degrade device performance. Based on this 3D array concept, NAND Flash scaling is expected to extend for a couple of technology nodes [7–9]. But in the end, it will run into the same problem as for the planar NAND, i.e. hitting the physical limitation of charge based memory devices and an intolerable increase in manufacturing cost.

Motivated by finding a successor of NAND Flash [10], many new technologies have been explored in the recent years to keep the pace with the increasing demand for high density, low cost and high performance memory applications. Novel memories, such as Ferroelectric Random Access Memory (FeRAM) [11], Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM) [12, 13], Phase Change Random Access Memory (PCRAM) [14, 15], Resistive Random Access Memory (RRAM) [16–21], etc are being investigated intensively (Fig.1.1). A comparison between the current and emerging memory technologies is listed in TABLE.1.1. All these emerging technologies demonstrate non-volatile memory behavior and promising characteristics such as fast Program/Erase (P/E) speed, low read and write energy consumption and excellent reliability (e.g. endurance, retention), etc.

Table 1.1: Comparison between the current and emerging memory technologies [22–26]

	Volatile		**Non-volatile Flash**		**Emerging non-volatile memories**			
						resistance modulation		
	SRAM	DRAM	NAND	NOR	FeRAM	PCRAM	STT-MRAM	RRAM
Configuration [a]	6T	1T1C	1T	1T	1T1C	1S1R	1T1R	(1S)1R
Cell Area (F^2)	140	6	5	10	22	4	10	4
P/E time (ns) [b]	0.3/0.3	<10/10	$10^6/10^5$	$10^6/10^7$	10/10	20/50	<10/10	>10/10
On/off resistance ratio						>10	~2	>10
Endurance	$>3*10^{16}$	$>3*10^{16}$	$>10^5$	$>10^5$	$>10^{14}$	$>10^8$	$>3*10^{16}$	$>10^{10}$
Retention	n.a	64ms	>10y	>10y	>10y	>10y	>10y	>10y
Energy/bit	~pJ	30fJ/ms	10-100pJ[c]	10-100pJ[c]	<0.1pJ	10pJ	~pJ	~pJ
Application	cache	Main memory	Storage	Storage	Storage	Storage	Main memory	Storage

[a] T:transistor S:two-terminal selector.
[b] Program/Erase.
[c] Per-page.

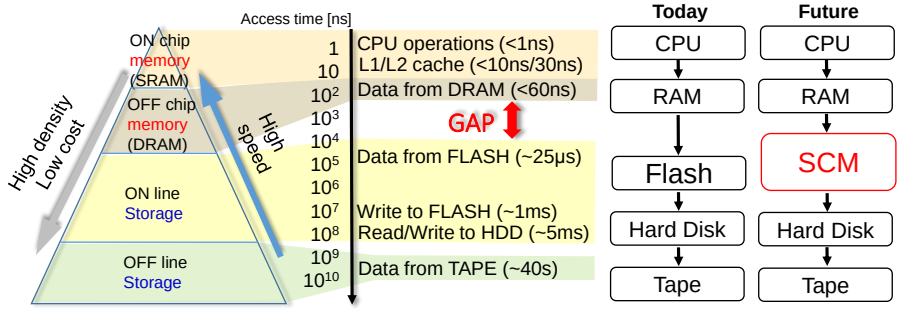


Figure 1.2: *Pyramid memory hierarchy in modern computer systems. Developed and emerging memory technologies are designed to bridge the access gap between memory-(main memory) and storage-type of memories. Reprinted from [10].*

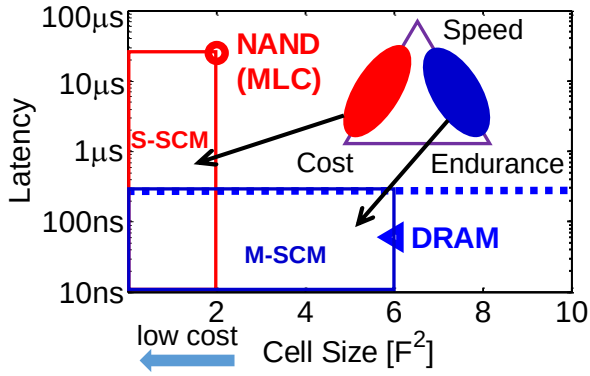


Figure 1.3: *Target requirements for S-SCM and M-SCM applications. MLC: multi-level cell, F:feature size. Reprinted from [10].*

Fig.1.2, the modern computer system needs memories to store information that requires immediate access (e.g. SRAM, DRAM), while it uses storage memories (e.g. NAND Flash, Hard Disk Drive, etc) to keep data that does not need at this specific moment, but can be required for the future usage. DRAM, typical for the main memory application, is well known for its high performance (e.g. fast access time) and low capacity (~Gb) due to its expensive fabrication cost. Storage memory, e.g. NAND Flash, offers much larger capacity than DRAM, while at the expense of lower performance.

Interestingly, investigation on the emerging memory technologies provides an opportunity for further improving the existing memory hierarchy in computer systems

nowadays [10]. The concept of Storage Class Memory (SCM) has been proposed [10, 27, 28], aiming to fill the access-time gap between NAND and DRAM, with a cost that would also lie in between that of DRAM and NAND Flash. This SCM class is further splitted in memory type (e.g. main memory) SCM (M-SCM) and storage type SCM (S-SCM). Fig.1.3 summarizes the performance target for both potential S-SCM and M-SCM applications. M-SCM focuses more on the performance, e.g. close to DRAM, but with less cost than DRAM. On the other hand, a low cost per bit (e.g. comparable to NAND) is more important for S-SCM, with extra benefit that S-SCM could offer a higher performance than NAND.

Among all the emerging memory technologies, STT-MRAM seems to be a good candidate for the M-SCM due to its fast access speed (<10ns), close-to infinite P/E endurance(>10^{16}), limited area consumption (10F^2) and low power operation (~pJ), which satisfy the most stringent requirements for the high performance memory applications. Moreover, due to its non-volatile behavior, STT-MRAM does not require a periodic refresh process, which is mandatory for DRAM. This further reduces the power consumption. On the other hand, RRAM seems to be the most promising candidate for the S-SCM applications, due to the following reasons:

- *Simple structure*: RRAM has very simple two-terminal Metal-Insulator-Metal (MIM) structure, which allows highly geometrical scalability.
- *Good Manufacturability*: RRAM uses fully CMOS compatible materials, which can be fabricated using fab-friendly processes. On the contrary, FeRAM, STT-MRAM and PCRAM require dedicated processes using ferroelectric, chalcogenide or magnetic materials.
- *Excellent scalability*: Resistive memory functional devices have been demonstrated down to 10x10nm^2 size [17], exceeding the physical limitations of the Flash memory. Furthermore, it has better scaling potential compared to STT-MRAM and FeRAM. The latter two memory technologies require complex material system for fabricating the functional devices.
- *Low cost per bit*: Implementation of RRAM in dense cross-point arrays can achieve the smallest cell footprint, i.e. 4F^2, with F being the feature size (i.e. half-metal pitch in memory technology). Moreover, a non-linear self-rectifying resistive memory (discuss later in the section 1.4) such as VMCO [29], is compatible with "BiCS" (Bit-Cost Scalable) 3D architecture (similar to that of 3D vertical NAND), allowing further cost reduction.
- *Multi-level cell*: Resistive memory can provide large on/off resistance ratio, which potentially enables Multi-level Cell operation, further reducing the cost per bit. On the contrary, a typical on/off resistance window for STT-MRAM is less than 2, which makes Multi-level cell nearly impossible.

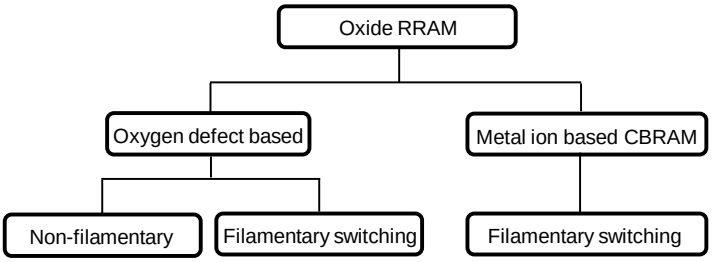


Figure 1.4: *Category of oxide based RRAM technology. Reprinted from [26].*

- *Fast P/E speed*: Program and Erase of resistive memory cells take much less time (>10ns) than that of Flash memory (>µs).

1.2 Resistive Random Access Memory

Resistive switching phenomena, with different underlying mechanisms, lay at the heart of most emerging memory technologies. For instance, the magnetic field is involved in the resistance change for STT-MRAM. For PCRAM, a thermal process is employed to control phase transitions between crystalline and amorphous in the chalcogenide material. The Resistive-RAM (RRAM) is the class of resistive switching memory technology occurring in metal-insulator-metal (MIM) structures. According to the defect type involved in the switching, resistive memory cells can be categorized into two groups, namely the oxygen vacancy based RRAM and the metal ions based conductive bridge memory (CBRAM). Furthermore, on the basis of different ways for modulating conduction by oxygen vacancies, filamentary and non-filamentary switching are possible (Fig.1.4).

1.2.1 Filamentary resistive switching

Most of oxygen-defect based RRAMs and all reported CBRAMs show filamentary switching. The resistive switching process typically includes three distinctive operations: Forming, SET, and RESET (Fig.1.5).

- *Forming*: This is a one-time step required to initialize the memory cell into the desired switching mode. After forming, a conductive filament is formed by creating a chain of oxygen vacancy (V_{ox}) defects in oxide or a chain of metal

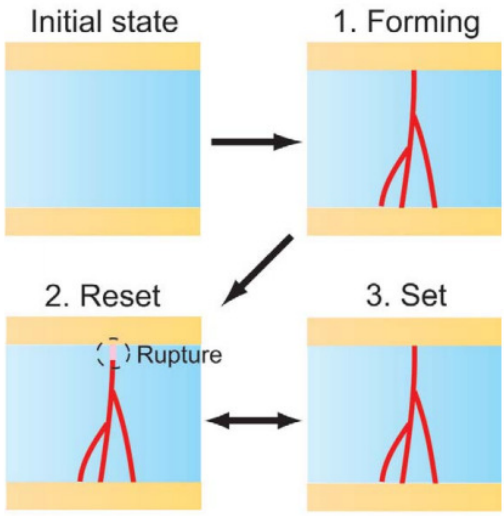


Figure 1.5: *Schematic of the as-fabricated state and after (1) forming (2) Reset and (3) Set process. Reprinted from [19].*

ions in CBRAM. After forming, the device is typically in the low resistance state (LRS).

- *RESET*: Rupture (or local thinning) of the conductive filament. After RESET, the memory device is in a high resistance state (HRS).
- *SET*: Restoration of the filament. After SET, the device restores the LRS.

The programming process can be achieved by applying DC voltage sweeps or voltage pulses. During forming and set operation, an external current compliance (CC) (e.g. using a semiconductor parameter analyzer, an transistor or a series resistor as the current limiter) is usually employed to reduce the RRAM switching current, to prevent overshooting current during the RESET operation [30] and permanent dielectric breakdown in the device.

According to the switching modes, most of RRAM devices can be classified into two categories: unipolar switching and bipolar switching RRAM. For unipolar switching devices, the resistive switching depends only on the amplitude of the applied voltage, regardless of the polarity of the applied voltage (e.g. SET/RESET can be done on the same polarity). If a unipolar RRAM shows SET/RESET switching for both polarities, it is also called as nonpolar RRAM [20]. A schematic of unipolar (nonpolar) switching behavior is sketched in Fig.1.6.(a). On the contrary, SET/RESET strongly depends on

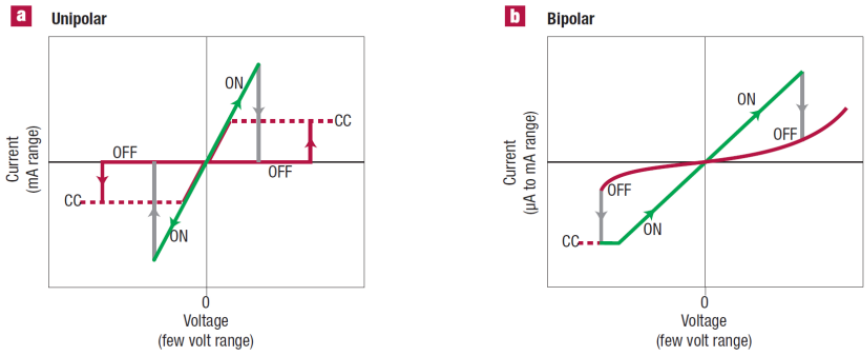


Figure 1.6: *Schematic of DC I-V characteristics of resistive memory in (a) unipolar switching mode and (b) bipolar switching mode. ON/OFF refers to low resistance and high resistance state, respectively. CC stands for current compliance. Reprinted from [21].*

polarity of the applied voltage for bipolar RRAM. If the SET occurs on one polarity, the RESET can only happen on the opposite polarity (Fig.1.6.b).

The interpretation for the Forming and SET in the oxygen-defect based RRAM seems reaching a consensus [20] that a dielectric soft breakdown is involved in these two processes [31] (For CBRAM devices, metal ions are injected to form conductive filament). However, the underlying RESET mechanism, which leads to the difference in bipolar and unipolar switching mode is still not very clear. A thermally driven process [32] is typically used to explain unipolar switching behavior, while oxygen (ions) migration model can explain parts of the bipolar switching observation [20, 26].

Filamentary resistive switching behavior is found among various transition metal oxides (TMO), some examples [33–42] are shown in TABLE.1.2. In addition to oxide materials, metal electrodes also play important role on the switching mode of RRAM. For instance, *Lin et al.* [39] reported ZrO_2 based RRAM with different electrodes (e.g. Pt and Ti). Even with the same oxide material, the switching mode can be different. In most cases, bipolar switching can be achieved by using oxidizable electrode such as Ti, Hf, TiN, etc, while unipolar switching is obtained by using inert electrodes (e.g. Pt) for both sides. In some cases, both unipolar and bipolar switching can be achieved on the same material system, e.g. TiN/HfO_2/Pt [40], depending on the polarity of the voltages which are applied to the device.

Although both unipolar and bipolar RRAM have received intensive study over the years, recently, research activities have been focusing on the bipolar switching mode RRAM for the following two reasons: firstly, the bipolar switching devices depending

Table 1.2: Switching modes for various metal-oxide based RRAM. Reprinted from [20].

Unipolar switching	**Bipolar switching**
Pt/NiO/Pt [33]	Pt/NiO/$SiRuO_3$ [36]
Pt/TiO_2/Pt [34]	Pt/TiO_2/TiN [37]
Pt/ZrO/Pt [35]	TiN/ZrO/Pt [38]
Pt/ZrO_2/Pt [39]	Ti/ZrO_2/Pt [39]
TiN/HfO_2/Pt [40]	TiN/HfO_2/Pt [40]
Pt/Al_2O_3/Pt [41]	Ti/Al_2O_3/Pt [42]

on the oxygen drift/migration requires less switching power compared to the unipolar devices. Unipolar switching needs thermally activated diffusion of the oxygen ions, which causes a relatively high RESET current. Secondly, oxygen ions migration based bipolar RRAMs always show better endurance than that of unipolar cells. However, the advantage of unipolar switching RRAM is that it can work with a simpler uni-directional selector, such as a PN diode (discussed later in Section 1.5.2.1).

1.2.2 Non-filamentary resistive switching

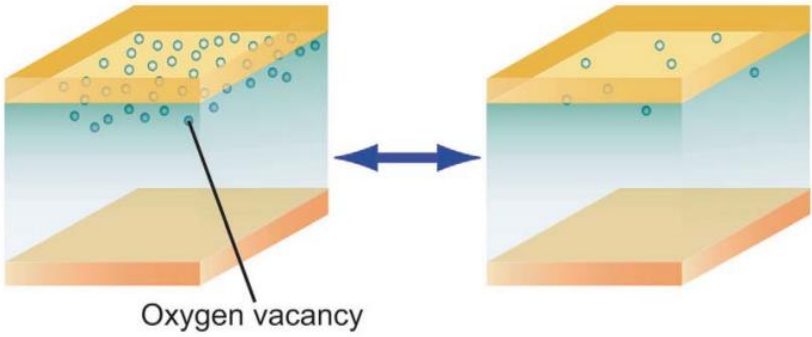


Figure 1.7: *Schematic of non-filamentary switching. Change of oxygen vacancy density at the switching interface. Reprinted from [19].*

In contrast to the filamentary RRAM, where the conductive path is formed locally (Fig.1.5), resistive switching that takes place across most of the device volume, or area, such as for example, at the interface between the metal electrode and oxide refers to

the nonfilamenary resistive switching memories. The resistance of a nonfilamentary resistive switching cell is inversely proportional to the device area after programming, while it is almost area independent for the filamentary switching devices.

A number of devices have been reported showing non-filamentary switching, based on physical mechanisms such as migration of oxygen vacancies (Fig.1.7) [29, 43] and trapping/de-trapping of charge carriers [44], etc. For instance, the defects (e.g. oxygen vacancies) can be moved back and forth with the polarity of the applied voltage [29], causing a change of barrier (at electrode/oxide interface) seen by the tunneling carriers. Thus, the change of resistance is due to the modulation of the defect profile. On the contrary, for a filamentary switching cell, the defects are generated and annihilated during the switching. Thus, an external current compliance is always required to avoid excess defect creation during the forming and SET process. This, however, is not necessary for the nonfilamentary resistive switching devices.

1.3 Cross-point RRAM arrays

1.3.1 Array configuration

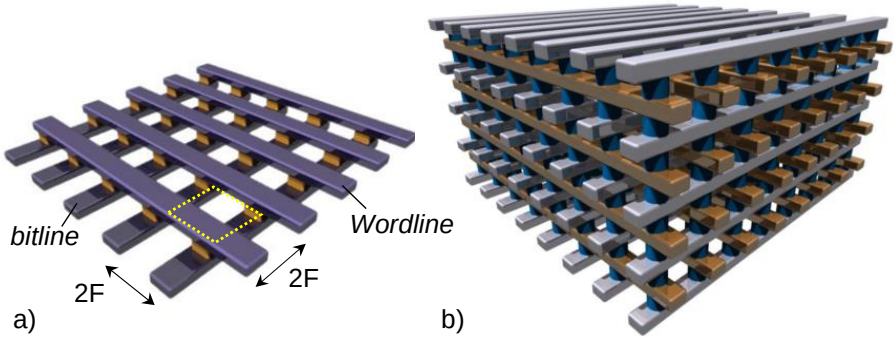
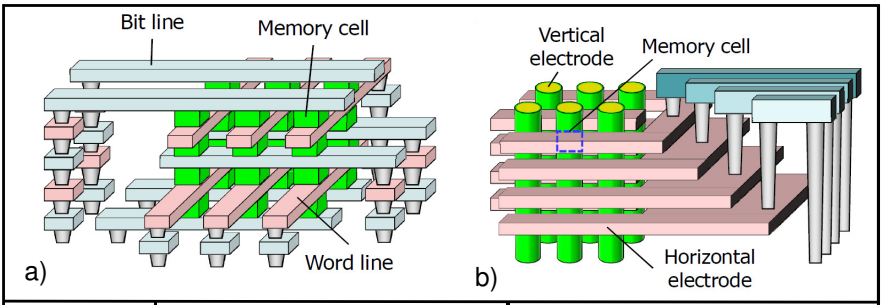


Figure 1.8: *Schematic of (a) 2D cross-point memory array. (b) stacked 3D cross-point array. Reprinted from [45].*

A simple two-terminal Metal-Insulator-Metal (MIM) structure allows the implementation of resistive memories into high dense cross-point arrays. The concept of "cross-point" for memory application can be traced back to more than 60 years ago [46]. A cross-point array consists of parallel interconnects (e.g. word lines/bit lines) at upper and lower planes, perpendicular to each other. Two-terminal memory devices are

implemented at the crossing points of these wires (Fig.1.8.a). Assuming the width of both lines and spaces equals F (the minimal feature size), this leads to an effective cell area being $4F^2$, yielding the smallest single layer cell footprint. It is feasible to stack multiple 2D layers into a 3D configuration (Fig.1.8.b). By doing this, the minimal feature size is reduced further to $4F^2/n$, where n is the number of stacking layers. This prompts stacked cross-point arrays to be a promising architecture for high density and large capacity memory arrays.

A practical problem associated with stacked 3D cross-point array is that the cost per bit does not always scale with the increasing number of layers, as it requires critical process steps, e.g. lithography and etch of metal lines and via contacts for each additional memory layer (Fig.1.9.a). This introduces extra process complexity and increases the fabrication cost. It has been reported that, to be most cost effective, the maximum number of stacking memory layers is about 8 [47]. In contrast, in the 3D vertical NAND (Bit-Cost Scalable) technology [6], a single critical lithography and etch step is used to define memory cells on different layers. Thus, such stacked 3D cross-point can hardly compete with 3D VNAND technology, from the cost point of view.



Merit:	Lateral scalability High cell efficiency	All memory layer formed at the same time Vertical scalability
Demerit:	One layer formed at a time Tight design rules necessary	Process complexity
Potential application:	Storage class memory (SCM)	Storage class memory (SCM) Post-NAND

Figure 1.9: *Schematic of (a) 3D stacked cross-point array. (b) Vertical cross-point array. Adapted from [47–49].*

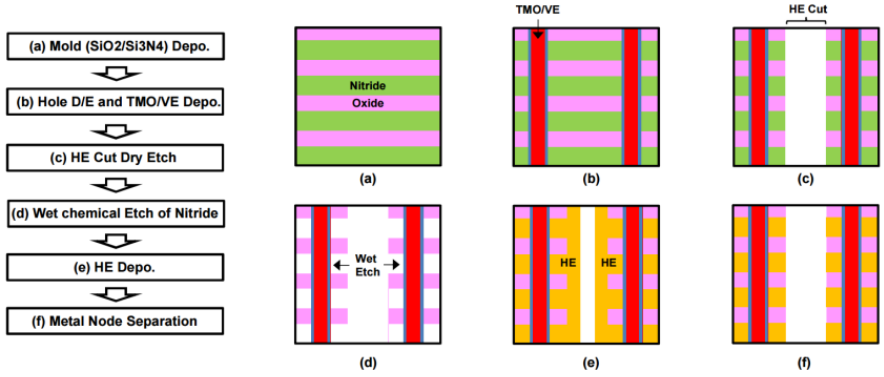


Figure 1.10: *Schematic of key process flow for vertical RRAM arrays (Fig.1.9.b). TMO: Transition Metal Oxide, HE/TE: Horizontal and Vertical Electrode. Reprinted from [47].*

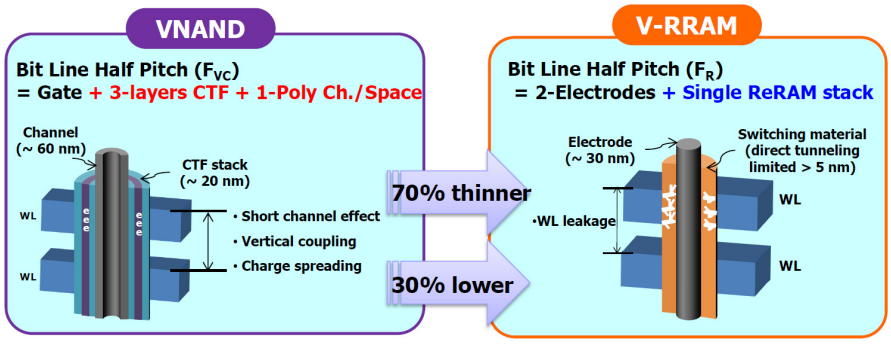


Figure 1.11: *Schematic of scaling potential for Vertical NAND and Vertical RRAM. CTF: charge trap Flash. Reprinted from [49].*

Recently, vertical cross-point arrays for RRAM (VRRAM) [47–49] were suggested (Fig.1.9.b), considering a similar approach BiCS (bit cost scalable) for 3D NAND Flash [6]. In this structure, all vertical cells on different layers are defined by a single critical lithography and etch step (Fig.1.10), for achieving comparable fabrication cost. On top of that, VRRAM is expected to have better scaling potential compared to VNAND [49] (Fig.1.11). Firstly, the lateral half-pitch of VRRAM is expected to be smaller than that of VNAND. The former is determined by the thickness of the RRAM device (simple metal-insulator-metal structure), while the latter is determined by the minimal poly Silicon vertical channel and charge trapping layer thickness.

Secondly, due to the short channel effect, vertical cell-to-cell coupling and change spread issue, a minimal horizontal word line (WL) to word line (WL) distance for VNAND is mandatory. For VRRAM, this distance is determined by the WL-to-WL parasitic leakages, which can be reduced when a good insulator barrier is employed. Considering these two factors, VRRAM is forecasted to consume less than ⅓ in lateral and ½ in vertical dimension compared to the current charge trap based VNAND, which is promising for further reducing the bit per cost. Therefore, 3D VRRAM is clearly a more suitable candidate than stacked 3D RRAM as the successor of VNAND Flash in the future.

1.3.2 Sneak current issue and solution

Although RRAM cross-point array and VRRAM shows promising potential for high-density memory applications, it has not yet been commercialized successfully today. One reason is that, to enable functional memory operation, it is required that each memory cell has good selectivity, which is enabled through a nonlinear electrical behavior. A strong non-linearity is essential to allow access to the specific device(s) in the memory array without affecting or being affected by the others [50].

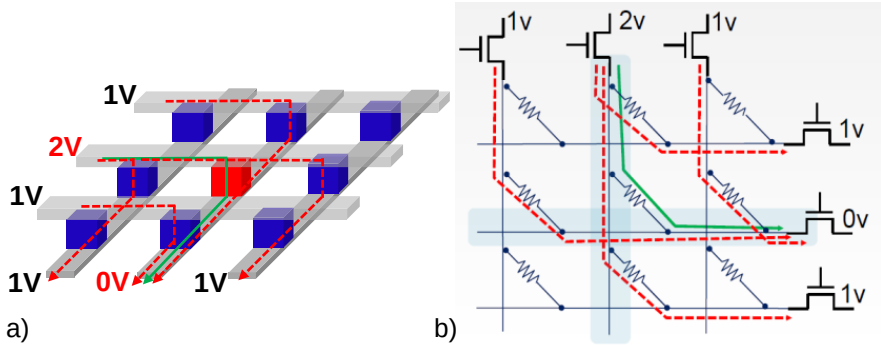


Figure 1.12: *(a) Illustration of sneak current in cross-point array with (nearly) linear resistive switching memory cells during read operation. (b) Circuit schematic of cross-point array. Red dash lines: sneak current paths. Green solid line: actual readout signal from the selected element. Reprinted from [45].*

However, most of the reported resistive memory cells show (nearly) Ohmic behavior in both LRS or HRS. This causes sneak currents through the unselected cells in the cross-point array during memory operation. Taking a 2D cross-point array as an example, read error occurs when the detectable difference between readout current of a selected

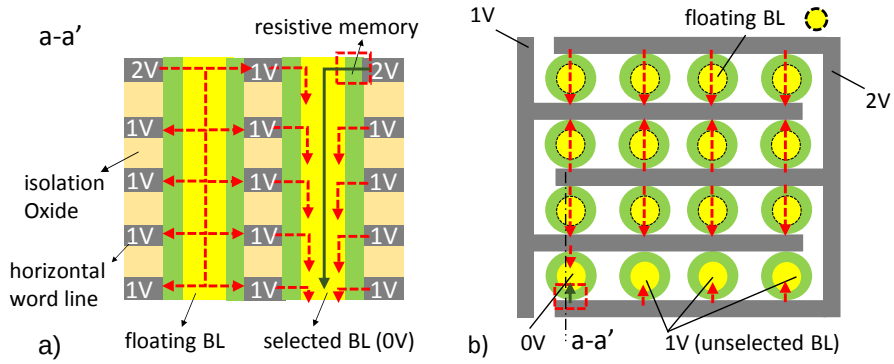


Figure 1.13: *Illustration of potential sneak currents in VRRAM array (Fig.1.9.b) with (nearly) linear resistive switching memory cells. (a) side view of cross-section a-a'. (b) top view. Red dash lines: potential sneak current paths. Green solid line: actual readout signal from the selected element.*

element in LRS and HRS vanishes (Fig.1.12). Due to the presence of the line resistance, the extra leakage induces significant IR voltage drop on the interconnecting lines, thus degrading the accessibility to the target cell, especially during the write operation where high currents are involved. Moreover, the leakage currents raise the total power consumption. With increasing array size, the array performance degradation is getting even worse due to the presence of more leakage paths. The sneak current issue occurs for vertical RRAM array as well (Fig.1.13) when linear resistive memory elements are used. These leakage currents would degrade array performance. For instance, the readout current (collected on the selected bitline pillar) consists of both real read signal and parasitic leakage currents from the unselected cells at different layers. With increasing the number of layers for VRRAM, more cells are connected to the vertical bitline pillar. This leads to more leakage paths, which causes additional read margin degradation (a detail analysis for VRRAM is presented in the Chapter 6).

In the ideal case, the memory operation (e.g. read and write) is supposed to take place only on the selected memory cell(s), leaving the rest of the cells unaffected [50]. This, results in zero parasitic leakages and no additional power dissipation. However, this is nearly impossible in reality. An alternative solution is to introduce non-linear I-V characteristics [50, 51] into each memory cell. To this end, a possibility is to use a separate, non-linear device, such as a diode [51], serially connected with each resistive memory element, in a one-selector one-resistor (1S1R) configuration (Fig.1.14). A two-terminal selector structure is required for implementing this in a cross-point array, so as not to cause additional memory array area overhead. In this case, the parasitic leakage is largely suppressed due to the high resistance of a non-linear selector at small

bias, which would dominate the full cell characteristics for the unselected memory cells.

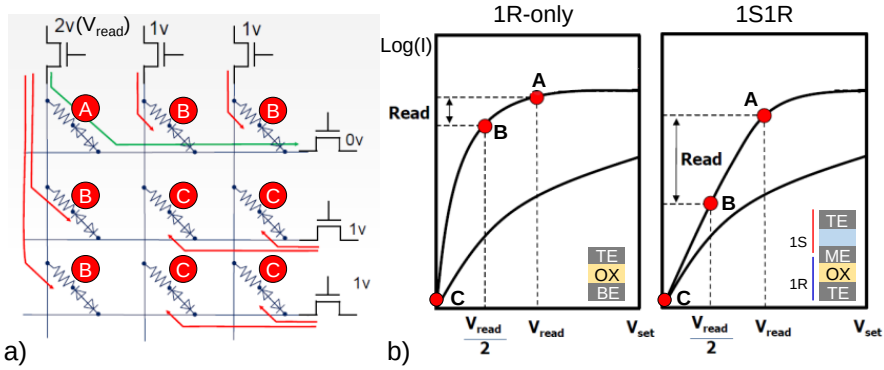


Figure 1.14: *(a) Schematic of leakage current suppression by introducing non-linear characteristics into each memory cell during read operation. (b) I-V comparison of (nearly-) ohmic 1R and non-linearity '1S +1R' cell configuration. TE: top electrode, ME: middle electrode BE: bottom electrode. Adapted from [45, 49].*

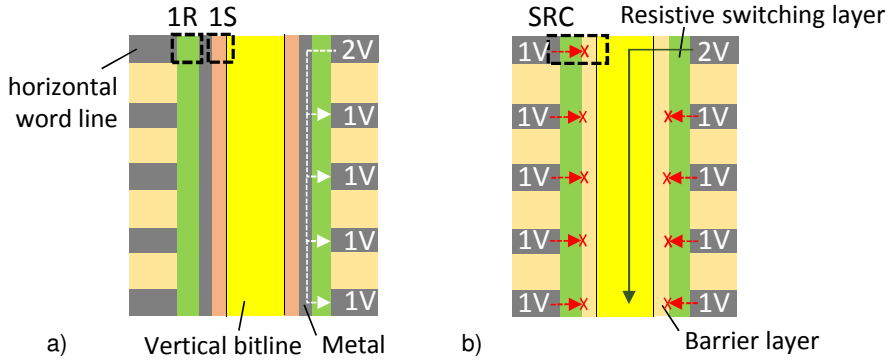


Figure 1.15: *(a) 1S1R configuration with inner metal electrode is not appropriate in VRRAM since it would form a conductive electrode connecting the cells on the same (vertical) string, creating additional short-circuit paths. (b) A non-linear self-rectifying cell (SRC) is suitable for VRRAM. e.g. to block the leakage currents by build-in tunneling barrier in the device. The arrows indicate the potential leakage paths.*

The advantage of this approach is that each of the elements can be tuned separately

Table 1.3: Comparison between 1S1R and SRC cell configuration

	One-selector one-resistor (1S1R)	**Self-rectifying cell (SRC)**
Merit	• Decouple control parameters, allow the optimization of individual component separately	• Easy process integration • Compatible with both stacked 3D cross-point array and vertical RRAM structure [a]
Demerit	• Increase process complexity, process compatibility between the two elements (e.g. thermal budget, etching chemistry, etc) • Not compatible with vertical RRAM structure	• Difficult to fulfill all the requirements from both memory and self-selectivity aspects

[a] Complementary switching cells [52–56] with inner metal electrode are not compatible with VRRAM.

to achieve the best full cell characteristics that fulfill the performance targets [50], while the disadvantage is the increasing process complexity required to integrate full stack. Moreover, if a middle electrode is needed between the 1S and 1R components, so as to form a M-X-M-I-M stack ('I': oxide for resistive memory, 'X': material for selector), the structure is not compatible with a vertical RRAM architecture (Fig.1.15.a). Firstly, it would compromise the lateral scaling. Secondly, it would form a conductive electrode connecting the cells on the same vertical string, thus creating a short between neighboring cells at the adjacent planes. To isolate the cells, this inner electrode must be etched away, which is almost impossible. Thus, a second approach is to directly introduce non-linear I-V behavior into the memory cell itself. Such resistive memory device is also called self-rectifying cell (SRC)[1] or selectorless memory device (we will discuss SRC in the section 1.4). In this case, only one memory device is needed to be integrated, without implementing a separate selection device. A non-linear SRC is compatible with VRRAM architecture (Fig.1.15.b) as well as planar cross-point arrays. This approach has an obvious advantage from process point of view, however, finding the proper material systems to achieve performance requirements from all aspects such as stable memory resistance states (LRS/HRS), high non-linearity for both read and write operations, low switching current and voltages, etc, remain big challenges. The pros and cons for both approaches are briefly summarized in TABLE.1.3.

[1]The term "rectifying" usually refers to the device which lets current flowing only in one direction, which is proper for describing unipolar operating RRAM behavior. For bipolar operation RRAM, these cells should be called high non-linear RRAM cells, in a more precise way.

1.4 Self-rectifying cell (SRC)

In general, a resistive memory device which provides selectivity inherently without using an additional selector is called SRC. Recently, several SRC concepts have been reported showing attractive characteristics. In this section, three types of SRCs are briefly introduced.

1.4.1 Complementary resistive switching

CRS [52] was firstly reported by *Linn et al*. Their CRS cell consists of two back-to-back connected CBRAM cells (a single CBRAM cell has similar bipolar switching characteristics to that of oxide-based RRAM). A conductive filament of copper-ions is formed (LRS) by applying positive voltage on the Cu electrode and dissolved (HRS) by applying voltage at the negative polarity (Fig.1.16.a-d). Two stacked CBRAM cells, sharing one common Cu electrode in the middle, forms a CRS device (Fig.1.16.e). A "butterfly" shape I-V characteristics (Fig.1.16.f) is observed, owing to the four combinations of resistance states between the two resistive memory elements (Fig.1.16.Table). After initializing the HRS/HRS ('OFF') state, the logic state '1' is represented by LRS (top-cell)/HRS(bottom-cell) state and HRS/LRS has the state '0'. The fourth state ('ON', LRS/LRS) is triggered during the read operation. The leakage current can be suppressed at both logic states ('0' and '1'), because at least one of the resistive elements is in the HRS.

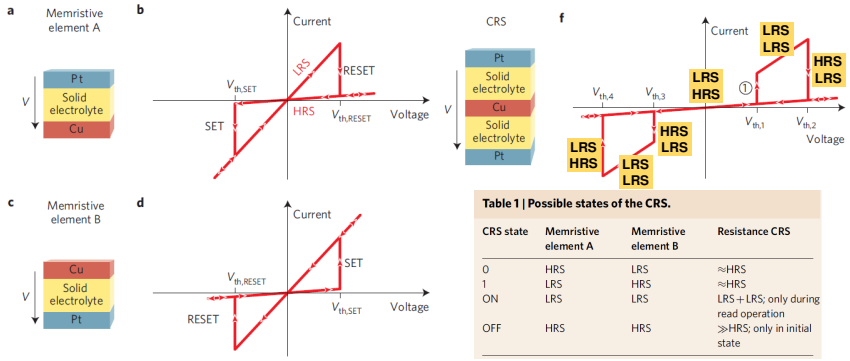


Table 1 | Possible states of the CRS.

CRS state	Memristive element A	Memristive element B	Resistance CRS
0	HRS	LRS	≈HRS
1	LRS	HRS	≈HRS
ON	LRS	LRS	LRS + LRS; only during read operation
OFF	HRS	HRS	≫HRS; only in initial state

Figure 1.16: *(a)-(d) Schematic of single CBRAM cell and typical switching characteristics. (e) Structure of CRS cell (f) Switching behavior of a CRS and illustration of resistance state distribution between the two CBRAM elements. Reprinted from [52].*

The logic state is distinguishable by applying a positive read voltage greater than the set voltage (V_{SET}) of the bottom cell. When the cell is in LRS/HRS (logic '1') state, this triggers the formation of a filament in the bottom cell, thus LRS/LRS is achieved, resulting in a high readout current. On the other hand, the cell stays in HRS/LRS (logic '0') at read voltage leading to a low readout current. The read '1' operation in the CRS cell is destructive, so a write-back process is needed to bring the LRS/LRS to the original LRS/HRS state by applying a negative voltage. This will increase the complexity from peripheral circuit design point of view [50]. Moreover, it causes extra power consumption, which makes it less attractive for frequently-read memory applications. Furthermore, this limits the read endurance to be equal to the program endurance.

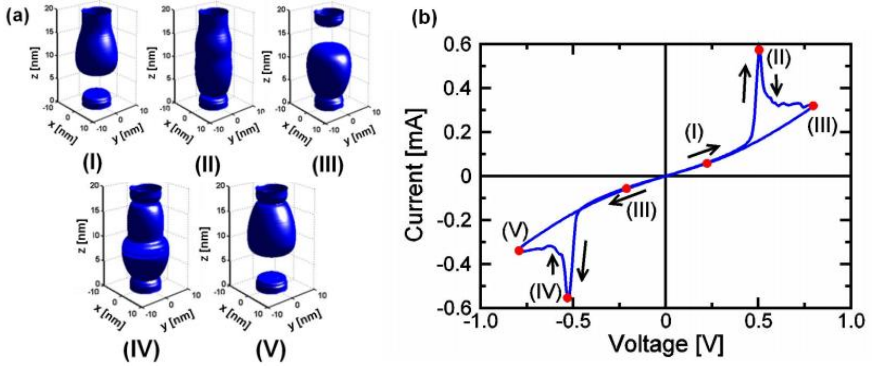


Figure 1.17: *(a) Simulated filament's shape and (b) corresponding I-V sweeps shows CRS behavior. Reprinted from [57].*

Until now, CRS have been reported not only for CBRAM [52, 53], but also for a variety of oxide-based RRAM [54–56] and amorphous carbon based RRAM cells [58], in a back-to-back connected cell configuration. However, the inner metal electrode makes the device structure less attractive to VRRAM architecture (Fig.1.15). In contrast to these M-I-M-I-M ('M': metal, 'I': insulator or electrolyte) CRS structure, *Nardi et al.* [57] reported CRS operation in single a HfO_x layer M-I-M stack (Fig.1.17). The CRS behavior in this case is explained as following [57]: in mode (I), a depletion gap (e.g. lack of oxygen vacancies) is created near the bottom electrode when a strong negative voltage (e.g. with respect to top electrode) is applied, thus the cell reaches the high resistance state; (II) when a positive voltage is applied, the oxygen vacancies are drifted towards bottom electrode and form conductive filament, the cell shows a low resistance state ; (III) further increasing the positive voltage causes depletion of oxygen vacancies near top electrode, leading to a high resistance state again. Thus, in the same way, the conductive filament can be re-connected (IV) and depleted (V) by

applying negative voltage [57]. Fig.1.17.(a) shows the simulated filament's shape by a numerical model and corresponding I-V characteristics during switching. Beyond simulation analysis, the paper also reported a real oxide-RRAM (TiN/HfO$_{x(5nm)}$/TiN) stack showing such CRS behavior, which aligns with the simulation prediction.

In summary, interests for CRS cells are driven by their non-linear I-V characteristics, which can be achieved using the existing bipolar resistive memory cells. However, several issues are remaining as challenges for practical CRS cell implementation. Firstly, it is hard to control the uniformity of CRS due to the variability inherent to each memory element in the stack. This implies that it could be difficult to achieve low current operation in the CRS, as the variability usually increases with lowering the current for the filamentary resistive elements [59–61]. Secondly, a destructive read requires a write-back process, which increases complexity of circuit design.

1.4.2 Hybrid RRAM-selector cell

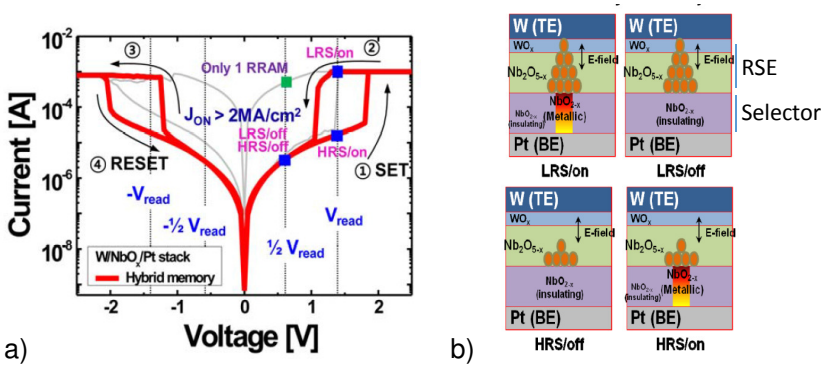


Figure 1.18: *(a) I-V characteristics of hybrid W/NbO$_x$/Pt device showing both threshold switching and resistive memory behavior. (b) Proposed switching model for hybrid resistive memory device. Reprinted from [62].*

A novel W/NbO$_x$/Pt cell was demonstrated by *Kim et al.* [62], where Nb$_2$O$_{5-x}$/NbO$_{2-x}$ stack layer is formed for a hybrid device with both memory and selector properties (Fig.1.18). Different properties are obtained due to different atomic ratio (Nb/O) in the NbO$_x$ film. For instance, a NbO$_{2-x}$ film [63] shows a typical metal-insulator-transition (MIT) [64] selector behavior, while Nb$_2$O$_{5-x}$/NbO$_{2-x}$ layer exhibits bipolar filamentary resistive switching. By controlling the oxygen concentration during deposition, Nb$_2$O$_{5-x}$/NbO$_{2-x}$ and NbO$_{2-x}$ are formed successively to achieve both

memory and selector functionalities in the same cell (Fig.1.18.b). A merit of this structure is that an additional middle electrode is not needed for separating the selector and memory cell. The reported hybrid devices show good DC cycling, high temperature thermal stability and good device-to-device uniformity.

1.4.3 Non-linear resistive memory with tunneling barrier

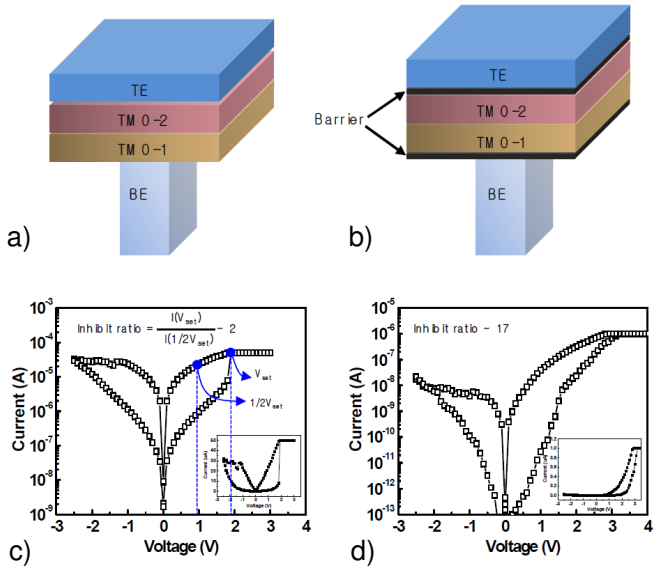


Figure 1.19: *Schematic of (a) the original resistive memory stack and (b) self-rectifying cell structure. (c) Switching characteristics of (a). (d) Low current and non-linearity is achieved for structure (b). Reprinted from [65].*

A non-linear resistive memory is also achieved by engineering the oxide multi-layers for filamentary resistive memories. For instance, where a thin tunneling barrier is inserted to generate non-linear characteristics [65, 66], *Park et al.* [65] reported a memory structure as shown in Fig.1.19. In this, the original resistive memory cell (Fig.1.19.a) consists of two transition metal oxide (TMO) films acting as resistive switching layers. While in the new structure, additional barrier layers are imposed at both bottom and top of the stack (Fig.1.19.b). Compared to the original cell switching (Fig.1.19.c), the new device exhibits strong non-linear I-V characteristics in the LRS (Fig.1.19.d). Moreover, the switching current is reduced to below ~1μA. Note that low current operation and high non-linearity are both desired for an ideal self-rectifying cell,

in order to minimize power dissipation and IR voltage drop during memory operation. Further investigation showed that the two inserted barrier layers (Fig.1.19.b) play different roles regarding to switching. The bottom barrier acts a tunneling barrier. The initial leakage current for both states can be decreased with increase of this barrier thickness, thus improving the cell non-linearity. The top barrier, on the other hand, provides self-current compliance. This improves pulse endurance by limiting potential current overshoot. As a consequence, excellent pulse stress up to 10^7 cycles at program condition was achieved with limited degradation through the whole I-V voltage range.

1.4.4 Vacancy Modulated Conductive Oxide (VMCO)-RRAM

Govoreanu et al. [29] demonstrated self-rectifying TiN/Al_2O_3/TiO_2/TiN cell (Fig.1.20). A post TiO_2 deposition anneal reduces the TiO_2 layer, creating an oxygen vacancy (V_o) profile across the film, hence a vacancy modulated conductive oxide (VMCO) active layer [29]. VMCO cell switches in self-compliance mode (e.g. no external current compliance is required). Furthermore, the cell exhibits low current operation and strongly non-linear I-V behavior. The switching current scales with cell size, indicating that the switching takes place uniformly over the entire cell area, in contrast to the filamentary resistive memory cells. The oxygen vacancies can move back and forth according to the polarity of the applied electric field [29], resulting in a change of the barrier seen by the tunneling electrons (Fig.1.21). For instance, in the HRS and initial state, the vacancies are close to TiN/TiO_2 interface, leaving the whole 'defect-free' tunneling barrier (e.g. Al_2O_3 + part of TiO_2) layer, thus increasing the cell resistance. When a positive voltage is applied on the top TiN, the oxygen vacancies are pushed through the whole TiO_2 region. Therefore, the LRS cell resistance reduces since it is mostly determined by the Al_2O_3 only.

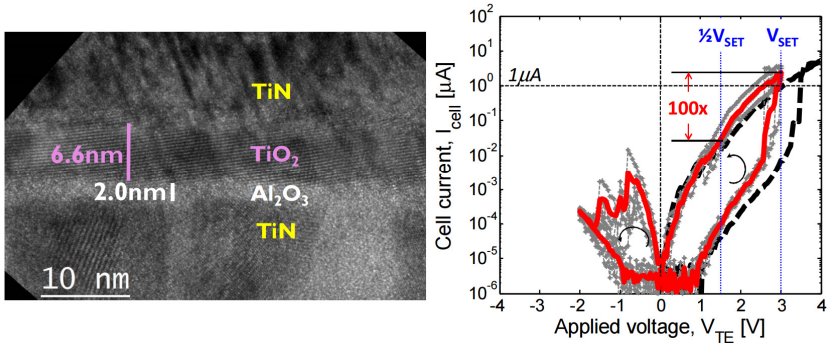


Figure 1.20: *(a) TEM picture of the proposed device structure. (b) Switching characteristics of VMCO cell. Reprinted from [29].*

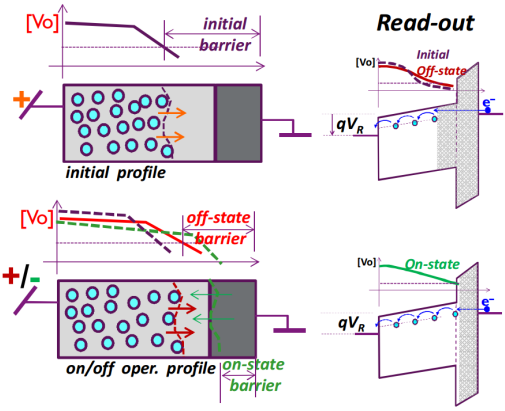


Figure 1.21: *Schematic of proposed model for VMCO switching. Reprinted from [29].*

Self-rectifying cell was also demonstrated by *Meyer et al.* [67] and *Siau et al.* [68]. A simple Pt/Tunneling oxide (TO)/Conductive metal oxide (CMO)/Pt stack was developed as a resistive memory device. Fig.1.22 (left) shows that self-compliance, low current switching and non-linearity can be achieved simultaneously. Although this cell structure is similar to that of the self-rectifying cells that we introduced before, the underlying resistance change mechanism is different. In this case, the resistance switching is controlled by the potential energy barrier modulation induced by the injection and removal of the oxygen ions (Fig.1.22, right).

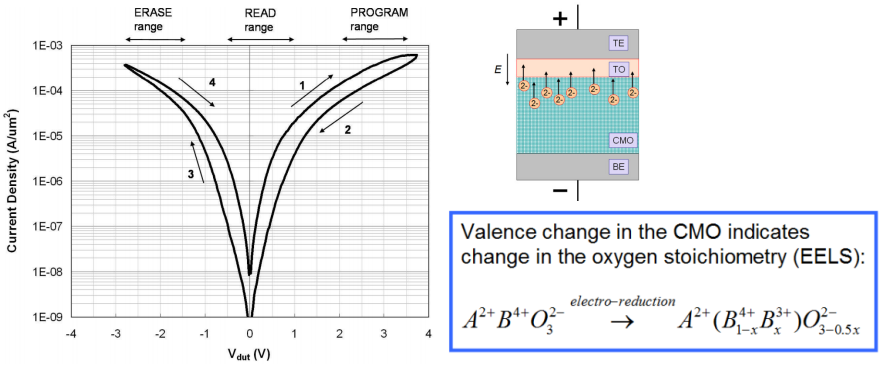


Figure 1.22: *(left) I-V characteristics of dual-layer resistive memory cell. (right) Proposed model for the resistance switching. Reprinted from [67, 68].*

1.4.5 Summary

TABLE 1.4 summarizes various SRC structures. Non-linear characteristics are mainly generated by using the concept of complementary resistive switching, additional tunneling barrier and a Schottky barrier, etc.

Interests for SRC originates from its simple structure. Most of the reported devices are compatible with VRRAM architecture, while the 1S1R cell configuration cannot fit for. To guarantee acceptable memory array performance, besides good memory properties (e.g. endurance and retention), SRC operating a low program/erase voltage (current) and having highly non-linearity for both read and write operations are required. However, it seems very difficult to achieve all these performance targets at the same time for a single device. The reported SRCs can hardly fulfill the requirements from both memory properties and self-selectivity aspects. Recently, with the success of 3D VNAND in the mass production and its continuous development, industry is considering the SRC technology (so as the VRRAM) being a long-term option for the VNAND successor.

Table 1.4: Reported SRC configurations and proposed mechanisms

SRC structure	**Switching Mechanism**
Pt/SiO_2/GeSe/Cu [52],Pt/SiO_2/Pt [53], TiN/HfOx/ZrOx/Zr [54], Pt/TaxO_{5-x}/TaO_{2-x}/Pt [55], TiN/HfO_2/Hf/TiN [56], Au/CNT/a-C/Au [58], TiN/HfOx/TiN [57]	Complementary resistive switching
BarrierA/TMO_1/TMO_2/BarrierB [65], TiN/Ta_2O_5/TiO_x/TiN [66]	Filamentary resistive switching + tunneling barrier
TiN/TiO_2/Al_2O_3/TiN [29]	Oxygen vacancy modulated (barrier tuning)
Pt/CMO/TO/Pt [67, 68], TiN/Ta_2O_5/TiO_x/TiN [69]	Oxygen ions modulated (Charge trapping/detrapping)
Pt/Al/PCMO/Pt [70]	Oxygen migration (AlO_x formation)
Cu/Cu-SiO_2/n-Si [71], Ni/HfO_x/n-Si [72], Pt/STNO(Nb-doped $SrTiO_3$)/Cu [73], Ag/a-S/p-Si [74, 75]	Reversed Schottky barrier formation

1.5 Selector for RRAM

Besides SRC, introducing an additional selection device in serially connected with each memory element in a 1S1R configuration is another effective way to inject self-selectivity to the cross-point arrays. Compared to the SRC, using separate memory and selector cell decouples control parameters, allowing optimization individual component separately to reach the overall device performance targets. As a consequence, the 1S1R device appears relatively easier to meet the performance requirements than the SRC.

It is believed that the 1S1R RRAM cross-point arrays, which are suitable for the potential storage class memory (SCM) applications, will pioneer the commercialization of the RRAM technology in the near future, before VRRAM acting as VNAND replacement.

Within the scope of this thesis work, we focus on the selector devices for the resistive memory in the 1S1R arrays. An ideal selector has several characteristic requirements to enable high density 1S1R cross-point arrays. These requirements are basically derived from circuit performance aspect, device and process compatibility.

In this section, we start with discussing some general requirements for the selectors, followed by the survey of different selector concepts reported so far.

1.5.1 Overview: general requirements for selector implementation

1) **Two-terminal structure**
   A two-terminal selector is needed so as not to cause extra memory array area overhead, to enable achieving the minimal single layer cell footprint $4F^2$ (F: feature size). This renders up the usage of a silicon-based four-terminal transistor as cross-point array selection device, although a transistor acts a perfect switch for blocking leakage current.

2) **High drive current**
   A selector should be able to provide enough current as needed for SET and RESET operations of the resistive memory cell. For instance, to enable resistive memory with ~10μA switching current, this translates to current density of ~10MA/cm^2 for a selector, where targeting 10x10nm^2 cell size.

3) **High non-linearity**
   The maximum achievable cross-point array block size depends on the circuit performance (e.g. sufficient read margin, acceptable read/write power, etc), which is strongly affected by the leakage currents from the unselected memory elements. The leakage current needs to be as low as possible [50] for improving

the overall memory operation. Considering that an ideal selector should have high current at high voltage ("pass" state, allows enough access voltage drops over the resistive memory element) as well as very small current at low voltages ("blocking" state) simultaneously, this translates into a highly non-linear characteristics [50].

4) **Bidirectional operation**
As most of the reported resistive memory cells exhibit better performance in bipolar operation mode, this requires a bidirectional selector, which could provide symmetrical I-V, such as high drive current and highly non-linearity at both polarities.[2]

5) **Voltage compatibility with resistive memory cell**
Resistive memory elements have various SET and RESET voltages depending on their material system and underlying working mechanisms. It is important that the selector element is compatible with the memory cell, in order to transfer selector non-linearity to the 1S1R full cell, to ensure limited leakage current from the unselected memory elements during both read and write operations. It is difficult to assess the performance of a selection device quantitatively without knowing the resistive memory to be paired [50, 76, 77]. For this reason, in the following selector survey, only qualitative assessment will be presented.

6) **Turn on/off speed and reliability**
An ideal selector device should be fast enough, imposing no speed limitation on the operation of the memory device. Moreover, the reliability such as cycling endurance, array yield, variability should be as good as or even better than the resistive memory cell [50].

7) **Process compatibility**
The material utilized by selector fabrication should be CMOS process compatible, which limits the usage of materials such as Pt, Ag, Au, etc in the structure. Moreover, to enable 3D stacked memory arrays, the thermal budget of selector device fabrication should be compatible with the back-end-of-line (BEOL) process. Besides, the selector should be able to withstand 400°C thermal stress for ~2hrs, considering the processes needed for stacking subsequent memory layers and wiring interconnects [50]. It is also desired that a selector has a simple structure and low aspect ratio, to reduce the process complexity.

The above discussed selector requirements make it very challenging to implement a qualified selector device for cross-point arrays. In the following part, we will survey the main reported selector concepts, and discuss their merits and demerits.

[2] In some cases, the term "rectifying" is used to describe selector non-linear behavior. For bidirectional selectors, "bidirectional rectification" should be used to emphasize that it is on both polarities.

1.5.2 Selector concept survey

1.5.2.1 Silicon-based selectors

Epitaxially grown PN (P-i-N) diodes [78–80] have been reported and demonstrated firstly for the unipolar phase change memories (PCRAM) as selector devices. *J.H.Oh et al.* [78] fabricated vertical diodes with selective-epitaxial-growth (SEG) on single-crystalline Si substrate, to improve the rectifying ability (forward/reversed biased I_{on}/I_{off} current ratio) compared to that of poly-Si case. The selector devices are integrated in a 512Mb PRCAM test chip (Fig.1.23.a) showing functional memory operations. The demonstrated PN diodes show high on-current density exceeding 25MA/cm^2 with I_{on}/I_{off} ratio of about 10^8. The advantage of using PN diodes as cross-point array selector devices come from three aspects: firstly, many decades of manufacturing and research experience with Si based device make it relatively easy for performance tunability, enabling PN diodes to be compatible with the memory cell [50]. Secondly, PN diodes provide high on-current, which is able to drive successful SET or RESET operation for the memory cell. Thirdly, parasitic leakage can be largely suppressed due to the extremely small reversed bias current.

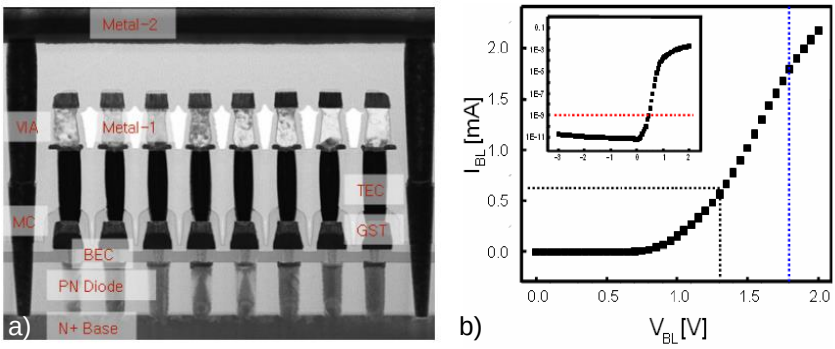


Figure 1.23: *(a) Vertical Si diode (90nm tech. node) selector for 512Mb PCRAM chip with 5.8F^2 cell size. BEC: bottom electrode contact. GST: $Ge_2Sb_2Te_5$. TEC: top electrode contact. (b) I-V characteristics for PN diode. Reprinted from [78].*

However, due to the fact that most of the resistive memories operate in bipolar switching mode, a unipolar PN diode is not suitable. Two-terminal Si-based selector being capable of providing symmetrical I-V characteristics have been reported, such as punchthrough NPN diodes [81–84]. The device concept reported in [81–83] is described as follows (Fig.1.24.a). A potential barrier is formed at N+/P junction to block the electrons to pass from one side to the other at zero and low bias. By increasing the applied

voltage, the depletion region of the P/N+ (cathode, reversed bias) extends and the P region becomes more attractive for electrons. This is an equivalent effect to reduce the barrier for electrons, which is similar to the "drain induced barrier lowering" (DIBL) or punchthrough effect in short channel transistors [50]. *Srinivasan et al.* [81] demonstrated NPN punchthrough selector (Fig.1.24.b) showing a maximum drive current density over 1MA/cm^2, with I_{on}/I_{off} ratio (half-bias nonlinearity) of about 4700. The operating voltage range is tunable, for instance, by adjusting the thickness of the P region and doping concentration. Fabrication of such diodes requires in-situ doped epitaxial Si growth process with thermal budget of over 700°C. The high temperature of process makes this concept less suitable for a BEOL process and 3D stacking.

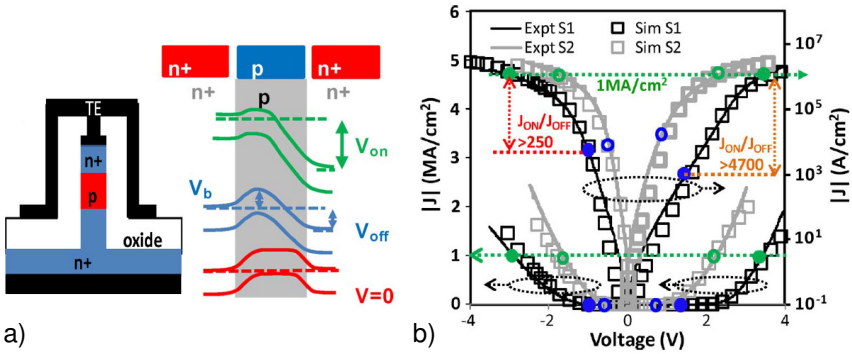


Figure 1.24: *(a) NPN selector structure and underlying conduction mechanism (b) Simulated and experimental I-V behavior of NPN selector. Reprinted from [81].*

Kim et al. [84] demonstrated a latch-up based NPN bidirectional selector. The silicon N/P/N regions are formed subsequently by three-step ion implantation, followed by the silicon pillar dry etching, resulting in a diameter size of 22nm (Fig.1.25.a). Interestingly, such device is characterized by an abrupt increase of current (Fig.1.25.c), in contrast to [81–83] showing a smooth I-V behavior. It is believed that excess holes are generated due to impact ionization at the reversely biased junction, and then are accumulated at the P (base) region [84]. These holes effectively reduce the barrier height for electrons injected from the emitter. This further enhances the process of impact ionization. Thus, a positive feedback loop is established, at certain level it results in a sudden jump of the current. This NPN selector show promising on-current exceeding 50MA/cm^2 and on-/off-state selectivity of over 10^4. While the thermal budget is not mentioned, it is expected that a high temperature annealing is necessary for dopant activation.

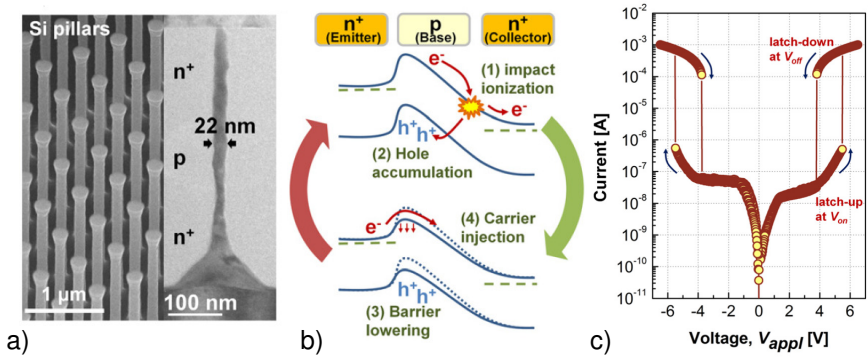


Figure 1.25: *(a) NPN pillar selector structure. (b) Proposed conduction mechanism (c) Experimental I-V behavior of NPN selector. Reprinted from [84].*

So far, we have introduced silicon-based two-terminal devices as potential selector applications. One common issue related to all silicon-based selectors remains the high temperature annealing process, which is required for dopant activation. This makes the devices less suitable for sub-400°C BEOL process and 3D stacked multi-layer memory structures. Besides, dopant and grain-size induced cell variability could be a potential issue for scaled devices, specifically to lowly doped and polycrystalline films, when device dimension becomes comparable to the grain size.

1.5.2.2 Metal-oxide-based selectors

a) Schottky diode

Various oxide-based Schottky diodes have been reported [85–90]. *Huang et al.* [85, 86] suggested a Ni/TiO_2/Ni structure showing bipolar non-linear characteristics (Fig.1.26.a). The proposed device has a maximum drive current of about 10^5A/cm^2 and an on/off ratio of about 10^6 (ratio between maximum current and current close to zero bias). The conduction mechanism is described as Schottky emission at the Ni/TiO_2 interface, where the extracted barrier height is ~0.55eV at zero bias (Fig.1.26.b). A non-linear Schottky diode is also fabricated using Pt/TiO_2/TiN by *Shin et al.* [87]. The device shows asymmetrical I-V behavior, e.g. lower current is observed when applying negative voltage on Pt electrode. This is explained by a higher Schottky barrier for electrons injected from Pt/TiO2 than that from TiN/TiO_2 interface. The maximum achievable current density is ~1.5*10^5A/cm^2, when injecting current from the TiN/TiO_2 interface.

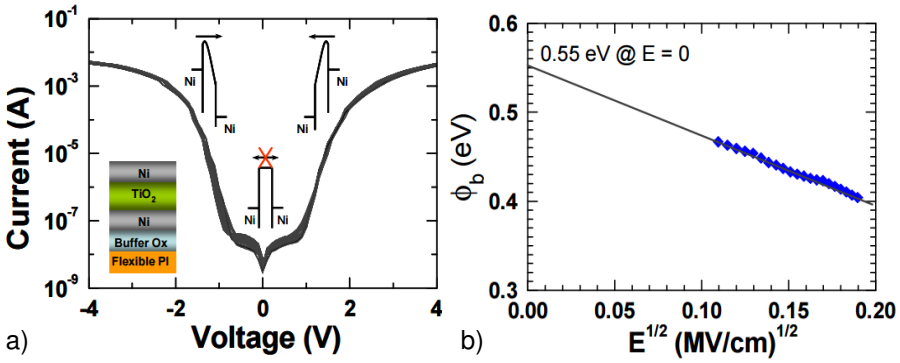


Figure 1.26: *(a) I-V characteristics for Ni/TiO_2/Ni selector. (b) Extrapolation of barrier height at Ni/TiO_2 interface. Reprinted from [86].*

By choosing a suitable metal electrode with respect to nitride-based semiconductor (SiN_x), a back-to-back Schottky diode is formed (Fig.1.27.a). The injection current is mainly determined by the reversed biased Schottky contact at the cathode, yielding non-linear I-V characteristics, which are tunable, e.g. by increasing the N% content to increase the band-gap of SiN_x, thus increasing the Schottky barrier height (Fig.1.27.b). With a N/Si ratio of ~0.3, the selector shows maximum current drive ~$2*10^5$A/cm^2 and an on/off ratio (e.g. half-bias current ratio) of ~150.

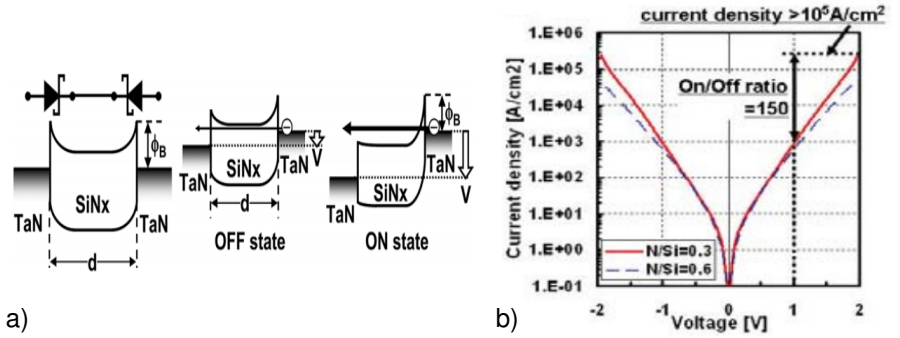


Figure 1.27: *(a) Schematic band diagram Metal/SiN_x/Metal Schottky selector. (b) I-V characteristics of selector. Reprinted from [89, 90].*

b) Tunneling diode

Another approach to achieve highly non-linear I-V characteristics is to use an oxide layer as tunneling barrier. Electron tunneling is a quantum-mechanical process that causes exponentially increasing current with the applied voltage [91]. A simple Metal-Insulator-Metal (MIM) consisting of thin oxide film such as HfO_2, Al_2O_3, TiO_2, etc [92, 93]. *Govoreanu et al.* [91] reported a novel TiN/Ta_2O_5/TiN bidirectional selector with an ultra-thin ALD deposited Ta_2O_5 layer, which achieves high drive current density ~10^5A/cm^2 , half-bias non-linearity ~360, fast turn-on/off speed and excellent AC endurance.

By engineering the tunneling barrier of using multiple oxide stacks [94–96], MIM selector has been optimized towards ~10^7A/cm^2 maximum drive current and half-bias nonlinearity of about 10^4 (Fig.1.28.a) in Pt/Ta_2O_5/TaO_x/TiO_2/Pt structure proposed by *Woo et al.* [95]. The oxide layers are formed by applying thermal oxidation annealing on TaO_x/TiO_2, resulting in formation of Ta_2O_5/TaO_x/TiO_2 stack (Fig.1.28.b). The outer oxide layer (i.e. Ta_2O_5 and TiO_2) provides large barrier height for electrons to be injected from both sides. Moreover, due to large total oxide thickness, the tunneling current at low bias is significantly suppressed. The barrier height gradually decreases towards the inner TaO_x layer (e.g. similar to a 'H' shape band diagram). At high biases, the current increases dramatically due to band bending, which enables electrons to tunnel through the thin oxide barrier at the injected interface. Instead of using a Pt electrode, a fully-CMOS process compatible W/Ta_2O_5/TaO_x/TiO_2/TiN device was demonstrated recently [96]. However, this comes at the cost of reducing cell non-linearity, possibly due to barrier height lowering given the low-workfunction metal (i.e. TiN).

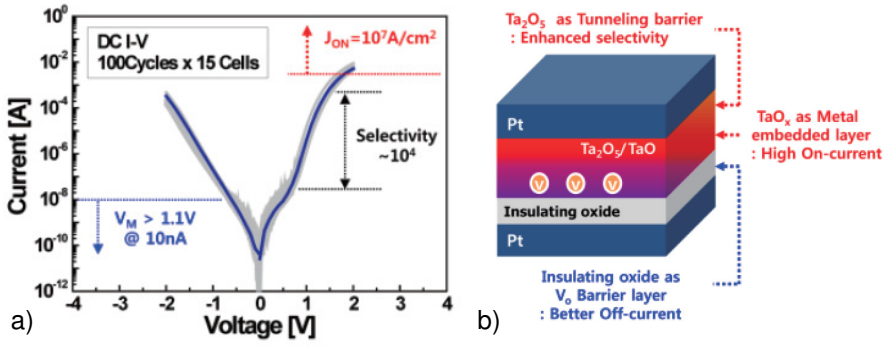


Figure 1.28: *(a) Schematic band diagram Metal/SiN_x/Metal Schottky selector. (b) I-V characteristics of selector. Reprinted from [95].*

1.5.2.2 Threshold switching (TS) selectors

a) Ovonic threshold switching (OTS)

Ovonic threshold switching (OTS) behavior [97] was firstly reported by *S.R.Ovshinsky*, in various amorphous chalcogenide alloy materials. A typical OTS I-V behavior is characterized by an abrupt increase of the current, for voltage-controlled sweeps. This corresponds to a S-type voltage snapback, with a negative differential resistance (NDR) between a threshold voltage and a holding voltage, for current controlled sweeps. The NDR region is unstable, and an abrupt and reversible transition occurs to either a high resistive state (off-state) or to a conductive state (on-state), Fig.1.29.

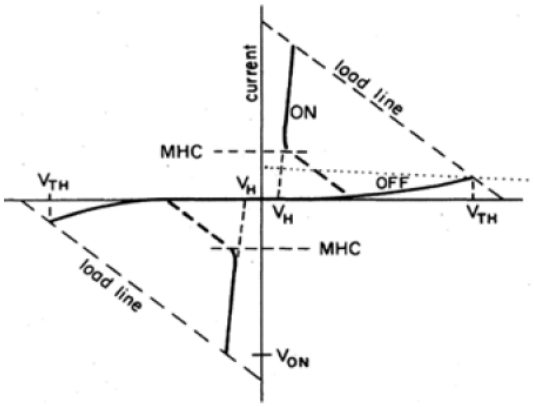


Figure 1.29: *Schematic of OTS characteristics. V_H: holding voltage. V_{TH}: threshold voltage. Reprinted from [97, 98].*

Interests for using the OTS mechanism for selector device implementation mainly comes from two aspects: firstly, its large off-state resistance ratio provides 1S1R full cell selectivity at program and readout conditions. Secondly, most threshold switching materials show high on-state drive currents (e.g. >10MA/cm^2), which enables resistive memory with over 10µA switching current at 10nm-scale.

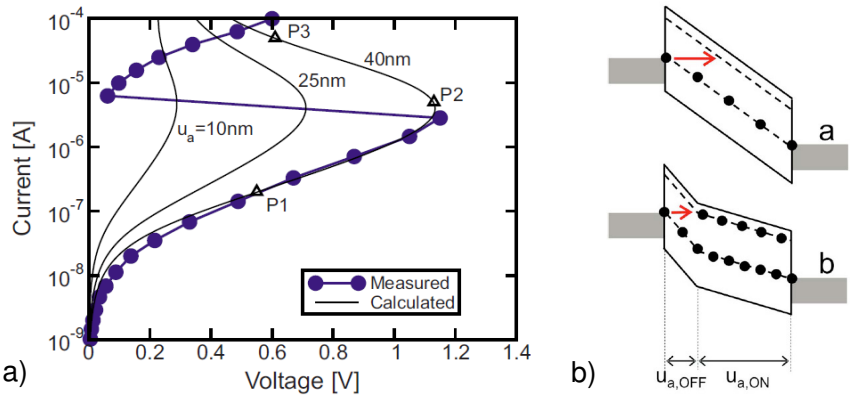


Figure 1.30: *(Left) Measured I-V sweep for amorphous $Ge_2Sb_2Te_5$ chalcogenide phase-change memory cell and analytical model prediction. (Right) Schematic for (a) low-voltage (off-state) region and (b) for high voltage (on-state) regime. Reprinted from [99, 100].*

The OTS phenomenon has been explained by several theories, such as thermally induced electronic switching [101], impact ionization and recombination [102, 103], etc. Recently, *Ielmini et al.* developed an analytical model based on trap-limited conduction [99, 100], which can fit with experimental data well (Fig.1.30.a). The I-V behavior at the low current regime is described by the Poole-Frenkel (PF) model, where an exponential increase of the current is due to the field-induced barrier lowering effect, which enhances electron hopping conduction. As further increasing the applied voltage, electrons tunnel to higher energy traps. The tunneled electrons occupy the shallow traps close to the conduction band, resulting in a non-uniformity of the electric field across the OTS material. To a certain extent, the region near the cathode becomes 'invisible' for the tunneling electrons, Fig.1.30.(b). This corresponds to the occurrence of the S-type I-V snapback and then OTS switching happens.

Several threshold switching selectors based on different chalcogenide alloy materials have been reported. *Lee et al.* demonstrated a structure of Ti/AsTeGeSiN/Ti [104, 105]. The reported selectors show limited degradation after applying alternative pulse voltage stress at on-state and off-state conditions up to 10^8 cycles, for both 30x30nm^2 and 0.5x0.5µm^2 cell sizes. The selector was successfully integrated with a TaO_x based resistive memory element (Fig.1.31.a), a clearly improvement on the low-bias leakage current can be observed in the full 1S1R cell configuration (Fig.1.31.b), with the on/off state non-linearity projected to ~100 at readout condition. The selector off-state leakage current can be further reduced by applying post deposition annealing. Such impact is well explained by a PF conduction model, where the trap density in the chalcogenide

alloy is strongly reduced after the thermal annealing [104].

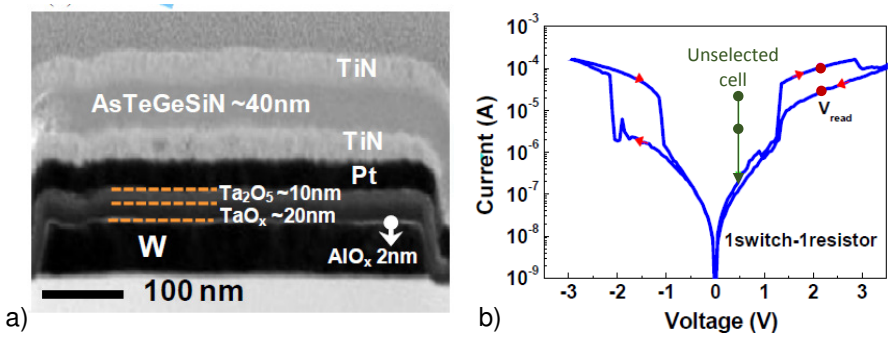


Figure 1.31: *(a) TEM picture of '1S +1R' device stack. (b) I-V sweeps of stacked 1S1R device. Inset: individual 1S, 1R cell behavior. Reprinted from [104].*

Kau et al. [106] implemented 1S1R cells of OTS selectors with unipolar phase change resistive memory (PCRAM) cells, Fig.1.32.(a). However, a linear scale I-V plot (Fig.1.32.b) makes it impossible to assess the selector off-state behaviors. To demonstrate functional array operation, the 1S1R cells were further implemented in a 64Mb cross-point test chip in 90nm CMOS technology. Single cell data show speed of ~9ns during RESET operation and endurance of 10^6 cycles. Statistical results on 2Mbit memory block show non-overlapping (~Δ1V) SET and RESET voltage distributions.

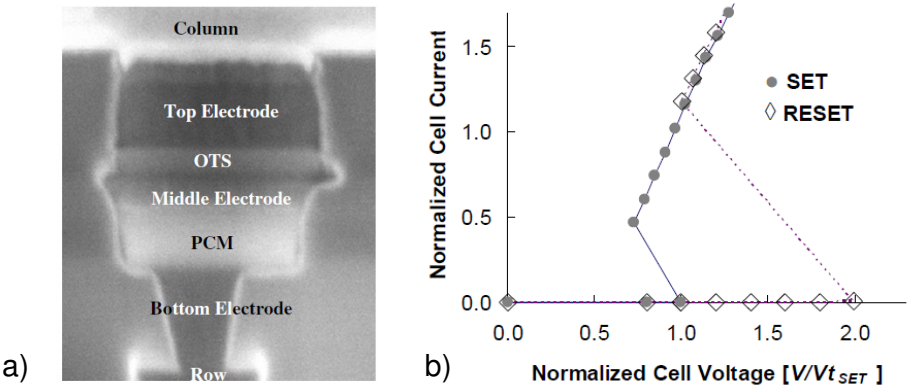


Figure 1.32: *(a) TEM picture of device stack. (b) I-V sweeps of stacked 1S1R device. Reprinted from [106].*

Chalcogenide alloy is an interesting material system for selector implementation given by its volatile OTS behavior. However, such volatile switching strongly depends on the alloy components and their concentration. With different alloy combination, non-volatile switching characteristics can also occur, e.g. Chalcogenide-based PCRAM cells, due to the local heat induced material crystallization effect. Thus, chalcogenide material composition has to be carefully tuned, so as the device shows only volatile switching for the selector applications. Next to it, the off-state leakage current should be minimized for selectors to cut-off the leakage paths. However, this can be very challenging to achieve given the large defect density in the amorphous alloy materials, which would enhance the PF conduction at low bias.

b) Metal-Insulator Transition (MIT)

Metal-Insulator-Transition (MIT) [64], is characterized by a fast, reversible transition between a low resistive metallic state and high resistive insulating state of an oxide. This transition is triggered electrically or thermoelectrically, and was observed in transition metal oxides such as VO_2, NbO_2, etc.

Son et al. presented Pt/VO_2/Pt selector [107] (Fig.1.33.a) showing moderate on/off non-linearity (~50), large drive current (>1MA/cm^2), excellent switching uniformity during 100 switching cycles (Fig.1.33.b) and fast switching speed (<20ns). The MIT behavior is only observed in small size devices, while the large-area devices show Ohmic I-V behavior (inset, Fig.1.33.a). This is possible due to the large defect density of the VO_2 layer, which increases the background leakage current. Although VO_2 exhibits excellent MIT behavior, its transition temperature is only around 67°C [62]. A too low switching temperature makes it less suitable for practical applications at operating temperature up to 85°C.

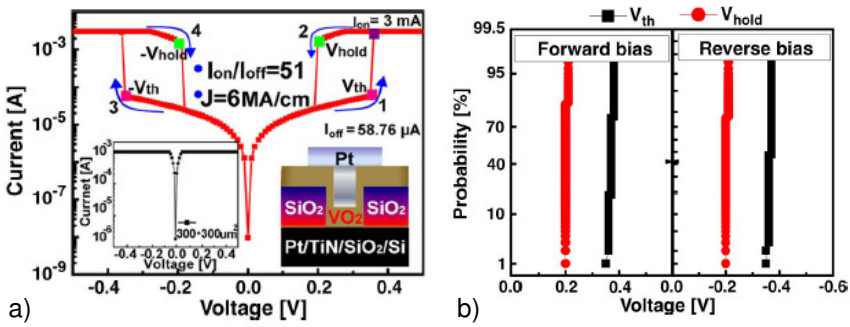


Figure 1.33: *(a) Typical threshold switching characteristics of Pt/VO_2/Pt selector in small 250nm hole structure. Inset: Linear I-V behavior of large micro-scale device. (b) CDF of threshold voltage (V_{th}) and hold voltage (V_{hold}) for 100 cycles. Reprinted from [107].*

In contrast to VO_2, NbO_2 based MIT selector remains stable up to 160°C. Similar to VO_2, Pt/NbO_2/Pt selector [62] shows excellent switching uniformity up to 1000 cycles (Fig.1.34.a). The threshold voltage and the hold voltages are relatively larger relative to that of VO_2-based device (Fig.1.34.b).

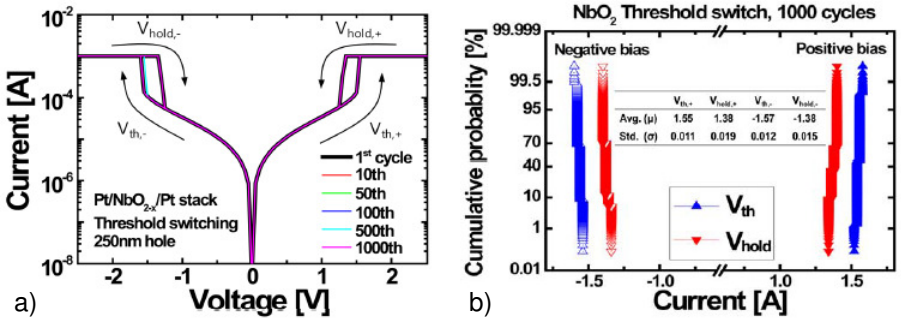


Figure 1.34: *(a) Threshold switching characteristics of Pt/NbO_{2-x}/Pt selector in 250nm hole . (b) CDF of V_{th} and V_{hold} during 1000 consecutive DC cycles. Reprinted from [62].*

A common concern for MIT based selectors is that the leakage current in the off-state is still very high. This can be attributed to the low band-gap specific to the MIT materials, which results in a low barrier height at the metal-oxide interface. On the other hand, such large off-state current is even necessary to enable Joule heating, as the transition is found to be thermally triggered in the reported cases.

c) Field Assisted Superlinear threshold (FAST) selector

Jo et al. [108] reported a Field Assisted Superlinear threshold (FAST) selector utilizing a superlinear threshold layer (SLT) where a conduction path is formed at the threshold voltage and disappears below a hold voltage (e.g. volatile filament), Fig.1.35. The threshold switching I-V behavior is characterized by an over 10^{10} non-linearity (100nmx100nm), large drive current density exceeding $5*10^6$A/cm^2, excellent endurance of over 10^8 cycles and fast turn-on and off time less than 50ns, etc. The FAST selectors are integrated with forming-free RRAM cells in a 4Mb 1S1R cross-point arrays. The integrated 1S1R cell shows >10^2 on/off-state resistance window and ~10^6 selectively (e.g. half-bias current ratio) for both read and write conditions (Fig.1.36). The process temperature of FAST selector is less than 300°C, which is suitable for 3D-stackable integration. In contrast to OTS and MIT based threshold switching selectors, FAST offers the largest on/off state current ratio. Although FAST selector shows excellent behaviors, the actual material system has not been revealed yet.

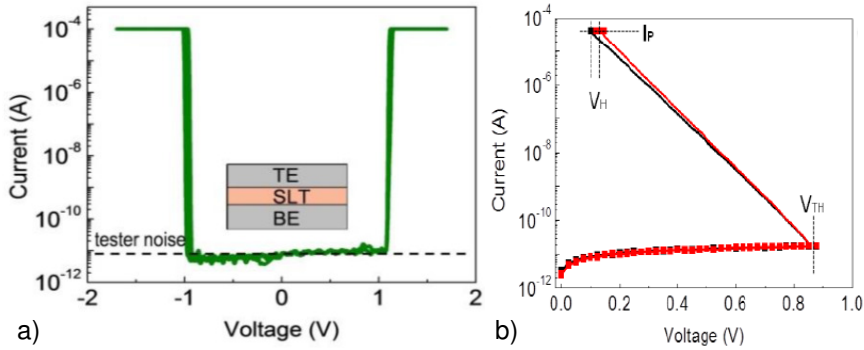


Figure 1.35: *(a) Voltage controlled I-V sweeps of FAST selector at 100nmx100nm cell size. SLT: superlinear threshold layer. (b) Current controlled I-V sweeps indicate negative differential resistance (NDR) between threshold voltage (V_{TH}) and a hold voltage (V_H). Reprinted from [108].*

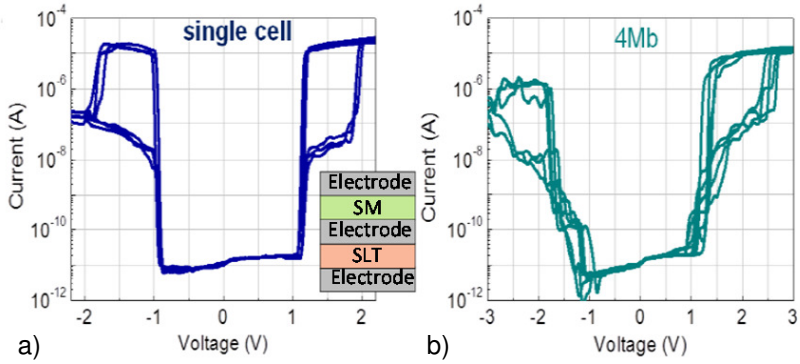


Figure 1.36: *Cross-point integration of RRAM devices with FAST selectors. (a) I-V sweeps of a single 1S1R device. (b) I-V characteristics of multiple cells in 4Mbit cross-point array . Reprinted from [108].*

1.5.2.3 Mixed Ionic-Electron Conduction (MIEC) selector

Mixed Ionic-Electron Conduction (MIEC) occurs in materials that conduct both electronic charges and ions. Recently, *Gopalakrishnan et al.* [109] reported selectors based on Cu-containing MIEC materials, where the MIEC layer is sandwiched between an inert bottom electrode (BEC) and top electrode (TEC). The applied voltage leads to

a transient Cu ion movement, followed by steady electron/hole diffusion current, which generates strong non-linear I-V characteristics. With an optimized CMP process [110–112], the integrated MIEC selectors in large 512x1024 arrays at 100% yield was achieved.

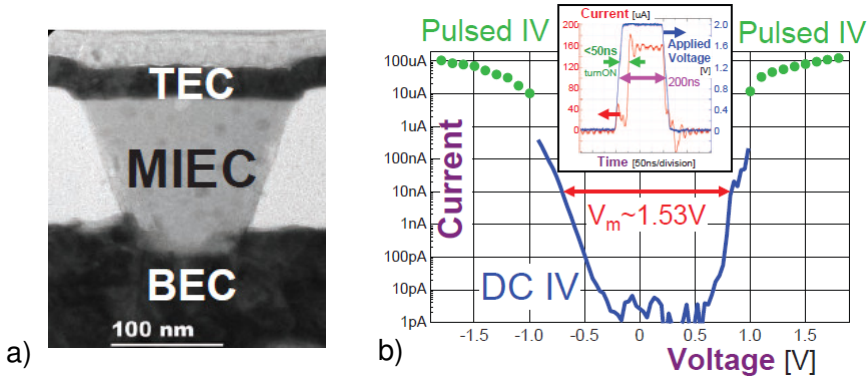


Figure 1.37: *(a) MIEC-based selectors with MIEC material sputter-deposited into a via hole, followed by CMP optimized process. (b) I-V characteristics of MIEC devices, the voltage margin (V_m) is defined as difference for reaching 10nA at positive/negative polarity. Reprinted from [110, 112].*

The MIEC devices were integrated using diode-in-via method [110] (Fig.1.37.a). Bipolar DC I-V characteristics show ~1pA leakage current near 0V and wide voltage range ~1.5V with below 10nA. Pulse measurements show that the MIEC devices can deliver maximum currents of over 100μA [112], which corresponds to a drive current density over 10MA/cm^2 for the reported selector size. Thus, MIEC based selectors can offer the desirable combination of low off leakage current and high on current. At low-current (<10μA) stress condition, the MIEC selector can withstand over 10^{10} endurance cycles [109, 110]. At high-current stress, the voltage margin (V_m) degrades and eventually the selector becomes short-circuited (Fig.1.38.b). TEM/EELS analysis implies endurance failure is possibly related to accumulation of Cu ions in the MIEC material (Fig.1.38.a).

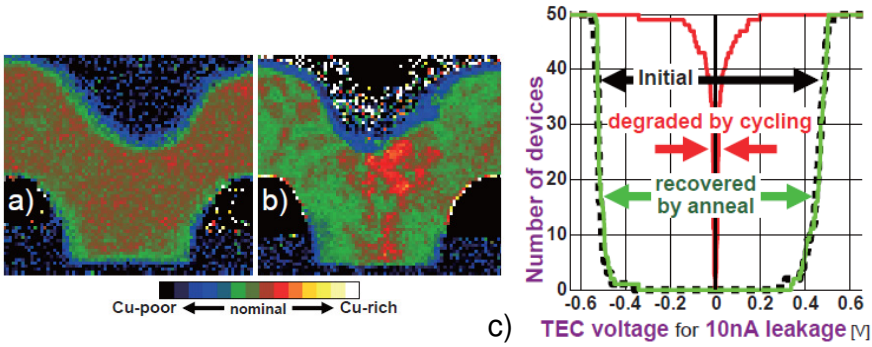


Figure 1.38: *Local stoichiometry from TEM/EELS of (a) as-fabricated and (b) after 425,000 cycles at 325*μ*A. Regions between TEC and BEC become Cu-rich. (c) Low bias leakage have been degraded after cycling, reflected by the close of the voltage margin . Reprinted from [110].*

Despite a Cu accumulation failure, another concern for MIEC-based selector is the low operating voltage range (or voltage margin). This makes MIEC selector less suitable for most of the resistive switching elements, which need to be programmed at relatively large voltages [76, 77].

1.5.3 Summary

A separate selector device providing extra nonlinearity to the resistive memory elements should offer ultralow off leakage currents when the memory cells are unselected, and provide sufficient on-current for enabling the switching of the selected cell. Table.1.5 [50] summarizes a qualitative benchmark table for the reported selectors so far. For J_{max}, '++' indicates the maximum drive current for reaching 10MA/cm^2, '+' is capable of delivering over 1MA/cm^2, while '-' marks the device fail to provide 1MA/cm^2. We simply define half-bias non-linearity (NL½) as the ratio between the maximum drive current (J_{max}) and the readout current at half of the voltage for reaching J_{max}. For the column of NL½, "++' indicates the current ratio larger than 10^5, '+' refers to the range between 10^3 and 10^5, '-' suggests that of less than 10^3. Symmetrical I-V selector is marked '+', otherwise '-'. For 3D integration, '+' indicates full 400°C BEOL compatibility, '-' suggests non-standard BEOL process which requires higher temperature.

To achieve high current, large non-linearity, good reliability under both device and process compatibility constraints remain challenge for selector device implementation.

Table 1.5: Summary of the reported selectors

	J_{max}	NL½	Bipolar	3D	other remarks
Si pn diode	++	++	-	-	suitable only for unipolar switching
Si npn diode	++	-	+	-	process complexity
npn threshold	++	+	+	-	process complexity
Schottky junction selector	-	-	+	+	easy for integration
Oxide multi-layer tunneling selector	++	+	+	+	unknown variability/scalability, Pt electrode.
Chalcogenide OTS	++	-	+	+	complex material system
MIT	++	-	+	+	low transition temperature
FAST	+	++	+	+	unknown material
MIEC	++	++	+	+	limited endurance, unknown material, voltage compatibility

1.6 Thesis content overview

1.6.1 Thesis objective

To realize high-density storage memory, RRAM arrays need a two-terminal selector device serial connected with each resistive memory element, to form a one-selector one-resistor (1S1R) configuration or, alternatively Self-Rectifying (selectorless) Cells (SRC), to suppress the parasitic leakage current.

Lots of work have been done in the past several years that investigated the RRAM technology and its potential for commercialization. Concerning the foreseeable big challenges in the SRC development, it is widely accepted that the SRC-based VRRAM will be a long-term option for VNAND replacement. It is most likely that the 1S1R RRAM cross-point arrays will lead the commercialization of RRAM technology in the near future, targeting the storage class memory (SCM) as potential applications.

However, several challenges remain for the 1S1R RRAM array development, one of the main issues is that a qualified selector element is still missing. To cater this

industrial and academic research interest for the RRAM technology, this Ph.D. study focuses on the electrical bit-cell analysis of 1S1R cross-point arrays, including two main objectives:

Firstly, we aim to make a quantitative assessment of various selector concepts and to provide engineering guidelines for selector device design. In this part, a SPICE-based top-down approach is employed to assess the required selector performance, depending on the particular choice of resistive switching element, considering the worst case scenario for the cross-point arrays. The selector requirements are derived by analyzing various bias conditions, taking into account several figures-of-merit to describe cross-point array functionality and performance.

Based on the initial simulation evaluation on selectors, the second objective of this thesis is to demonstrate a practical selector device that meets the target performance requirements, and allows fabrication in a CMOS compatible process. An amorphous silicon (a-Si) based Metal-Silicon-Metal (MSM) device is proposed as a promising candidate showing excellent electrical performance. Based on in-depth understanding for its underlying conduction mechanism, reliability and tradeoffs, several improvements have been achieved on MSM selector towards the target specifications.

1.6.2 Thesis outline

This thesis is arranged with the following chapters (Fig.1.39),

Chapter 2: MATLAB-based simulation framework for 1S1R cross-point array analysis

This chapter introduces a MATLAB-based cross-point array analysis framework. The simulation framework includes an effective SPICE circuit model, which provides an efficient and accurate way to quantitatively analyze the relationship between the cell characteristics and the cross-point array performance. This tool stands at the basis of the research work reported late in the thesis.

Chapter 3: Extraction of ideal behavior of selector (1S) and resistive memory element (1R)

Based on the analysis framework (introduced in the chapter 2), a comprehensive circuit-level simulation is performed to investigate the impact of 1S and 1R characteristics on the overall cross-point array performance. We derive the cell requirements using a top-down approach. The requirements that the 1S and 1R cell elements need to fulfill are extracted, considering sets of figures-of-merits describing the array functionality and performance. This circuit-to-device interaction analysis enables evaluation of

various selector concepts. Furthermore, it provides an engineering guideline for the 1S1R implementation.

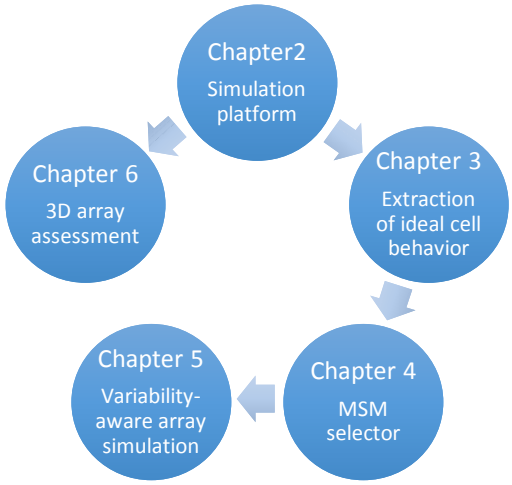


Figure 1.39: *Flow graph for each chapter.*

Chapter 4: Metal/Amorphous-Silicon/Metal (MSM) selector implementation

On the basis of the selector performance targets as extracted in the chapter 3, in this chapter, a novel Metal/Silicon/Metal (MSM) selector using ultra-thin undoped amorphous silicon (a-Si) is proposed for resistive-RAM selector applications. Based on an in-depth understanding of the conduction mechanism, several optimized MSM structures are proposed, of which performance are improved by both energy barrier modification and process engineering. Furthermore, a detailed reliability study is carried out, pointing out that the defect generation in the amorphous silicon layer may be responsible for selector degradation.

Chapter 5: Impact of device variability on the 1S1R array performance

In this chapter, a variability-aware 1S1R array performance assessment methodology is proposed, which accounts for both selector and RSE variability, as well as for the data pattern randomness. By injecting selector variability using the experimental data from our reference MSM selector (as discussed in the chapter 4), our analysis points out that the selector element is an important array variability contributor, degrading the overall read performance. Therefore, an additional margin in selector NL½ and a minimal 1R tail-to-tail resistance window (RW) are required to accommodate selector variability and to guarantee acceptable read performance.

Chapter 6: 3D RRAM

In this part, we improve the 2D cross-point array analysis framework and extend the capability for quantitative analysis of 3D RRAM, mainly focusing on the electrical behavior of Vertical-RRAM (VRRAM). A SPICE circuit model is developed for evaluating read and write performance of VRRAM, similar to that employed for 2D cross-point arrays. Finally, a comparison is made between stacked 3D RRAM and VRRAM arrays.

Chapter 7: Conclusion and outlook

The final chapter summarizes the main results and contributions of this thesis to the RRAM cross-point array research field. Finally, suggestions for future work are briefly discussed.

Chapter 2

MATLAB-based simulation framework for 1S1R cross-point array analysis

2.1 Introduction

Dense cross-point memory arrays require nonlinear cell characteristics to reduce the sneak leakage currents during memory cell operation [51]. Memory cell concepts either using a separate selector element or Self-Rectifying (selectorless) cells have been proposed. Although they are conceptually effective, it remains questionable to what extent they improve the array performance. Several papers have studied the impact of the cell behavior on the overall cross-point array performance using analytical approaches. However, the accuracy of these approaches [113–115] is limited due to over-simplified assumptions (e.g. device characteristics, excluding wire resistance, etc). To enable a reliable circuit-device interaction study, analysis based on circuit simulations will be employed.

In this chapter, a MATLAB-based cross-point analysis framework is presented. The framework includes an effective SPICE circuit model, which provides an efficient and accurate way to quantitatively analyze the relationship between the cell characteristics and memory array performance.

This chapter is organized as follows: in section 2.2, we review the basics of the cross-point memory architectures. The strategy for reading and writing the memory device in the array, the figures-of-merit for the memory operation, the worst case scenario and

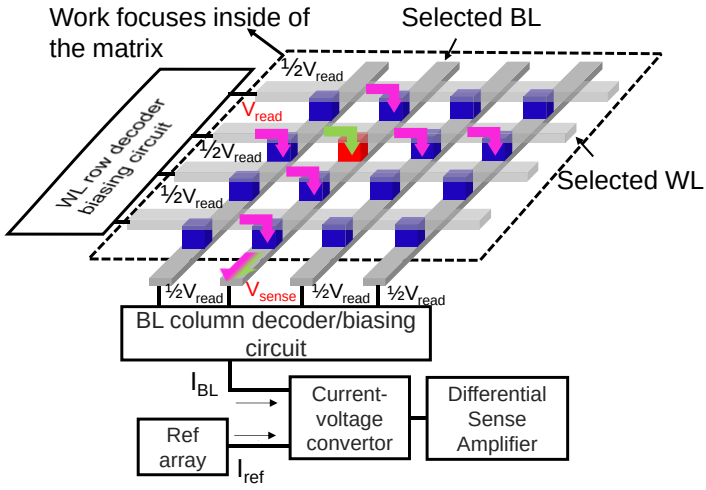


Figure 2.1: *Schematic of cross-point array under read operation using ½-bias scheme. Memory cells are located at each cross-point of the WL_s and BL_s. In a single-bit operation, only one cell (red) located at cross-point of the selected WL and selected BL is chosen for reading, while the unselected cells are partially biased. The arrows (purple) indicate the most relevant leakage paths for the read performance degradation.*

the bias schemes are discussed. In section 2.3, the 1S1R simulation framework will be introduced. The final conclusion of this chapter is summarized in the section 2.4.

2.2 Fundamentals of cross-point memory array

The schematic of a cross-point array is shown in Fig.2.1. The memory cell, defined by the cross-point region of a word-line (WL) and bit-line (BL), can be either a combination of non-linear selector and resistive switching element (1S1R) or a self-rectifying memory structure. The cross-point structure allows random access to any bit in the memory matrix or a parallel program and read operation for the bits along a single WL. However, the parallel operation within a local arrays remains questionable for resistive cross-point array due to the presence of the potential parasitic leakages [113]. Therefore, in our analysis, one bit per full local matrix is assumed to be selected and only one selected cell can be written or read at a time.

2.2.1 Read operation

In the read operation, the current sensing scheme [116, 117] is proposed as an efficient readout method for cross-point array, due to its low latency compared to the others [116], e.g. current-in voltage sensing and voltage-divider sensing schemes. In the current sensing mode, the selected cell state is discriminated by measuring the total current along the selected bit line (BL), when a read voltage (V_{read}) is applied on the selected WL while all the unselected WLs and BLs are partially biased. As an illustration, in the half-bias (½-bias) scheme, the unselected lines are biased at ½V_{read}. In a real memory array, to enable fast sensing [118], the selected BL and reference array (Ref array) are firstly charged up to a sense voltage (V_{sense}) during signal development phase, ensuring identical inputs for differential sense amplifier. The reference array block is a replica of bit line bias circuity, to guarantee the dummy cell in the reference array and the cell in the memory array has the exactly same bias conditions. Afterwards, the equalization is released, the BL readout current changes the differential voltage until the signal is large enough for the sense amplifier to detect, e.g. 100mV [118] to overcome the background thermal noise. To put it simple, the sensing circuit outputs either a logic '0' (cell in the HRS) or a logic '1' (cell in the LRS) depending on whether the BL readout current is larger or lower than the reference.

Several works have been reported achieving megabit (giga) test chips and prototypes [68, 89, 90, 119] for RRAM cross-point arrays. Given the various resistive memory cell behaviors, cross-point array peripheral circuits need to be designed specifically according to the cell characteristics. Within the scope of this Ph.D. study, the peripheral circuity design is not included at this stage. To assess cross-point array read performance, a simplified current-based definition of the **read margin (RM)** is employed as the figure-of-merit (FOM) for the read operation. This parameter measures the relative weight on the selected BL readout current when the selected cell is in different states. The RM can be defined as follows,

$$RM = \frac{\Delta I}{I_{ref}} = \frac{I_{BL(LRS)} - I_{BL(HRS)}}{I_{BL(LRS)}} \cdot 100[\%] \tag{2.1}$$

where $I_{BL(LRS)}$ is the current on the selected BL when the selected cell is in the LRS, while $I_{BL(HRS)}$ is the BL readout current when the cell is in the HRS. A reference current I_{ref} is chosen as I_{BL} for reading the LRS. The RM is strongly affected by the sneak current flowing through the selected BL. When the leakage current becomes the dominating contributor to the total readout current over the selected BL, read error occurs since the RM (ΔI) diminishes to zero, i.e. $I_{BL(HRS)} \approx I_{BL(LRS)}$.

Besides, the **read power (P_R)** is another important parameter during memory operation. We simply define (P_R) as the total power consumed from all voltage sources, which

can be calculated as,

$$P_R = V_{WLs} \cdot I_{WLs} + n \cdot (V_{WLns} \cdot I_{WLns}) + V_{BLs} \cdot I_{BLs} + n \cdot (V_{BLns} \cdot I_{BLns}) [W] \quad (2.2)$$

where WL_s and BL_s represent the selected WL and BL, while WL_{ns} and BL_{ns} stand for the unselected WL_s and BL_s, respectively. 'n' refers to the number of unselected WL_s and BL_s (e.g. assuming square shape array).

2.2.2 Write operation

The schematic of the write operation in the cross-point array under ½-bias scheme is illustrated in Fig.2.2. The program voltage (V_{dd}) is applied on the selected WL, while the selected BL is grounded to enable a successful write operation for the selected cell. However, a parasitic resistance effect becomes significant in the write operation since high voltages and currents are involved, relative to the read operation. As a result, the sneak current through the unselected cells causes extra voltage drop over the lines (i.e. selected WL and BL), which degrades the accessibility to a specific cell in the array since a smaller access voltage is effectively transferred to the cell. Raising the voltage on the selected WL being larger than V_{dd} to compensate the voltage drop effect is suggested. Consequently, the unselected devices at the beginning of the line may be accidentally mis-programmed, i.e. write disturbance occurs.

For an array to be functional, the voltage drop due to the finite lines resistance must be minimized. To measure the voltage transfer along the selected interconnects, a voltage-based definition of the **write margin (WM)** is used as figure-of-merit for the write operation. The WM is defined as follows:

$$WM = \frac{V_{access}}{V_{dd}} \cdot 100[\%] \quad (2.3)$$

where V_{access} is the voltage seen by the selected device, when V_{dd} is applied.

The **write power (P_W)** consumption is employed as another FOM for the write operation, which has a definition similar to that of P_R, eq.(2.2).

2.2.3 Worst case scenario

The cross-point array performance strongly depends on the selected cell location and array data pattern [114]. In this work, we adopt a worst-case scenario, which is further described below.

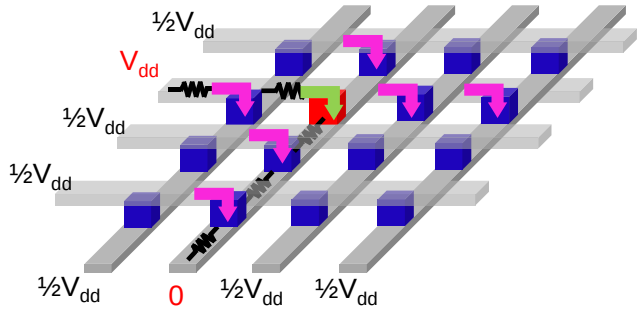


Figure 2.2: *Schematic of cross-point array under write operation using ½-bias scheme. Selected cell (red) biased between V_{dd} and 0V is selected for writing. Arrows (purple) indicate the potential leakage paths. Note that: the line resistances only located at the most relevant paths for WM degradation are indicted.*

a) Worst case cell location

The worst selected cell position is the one located at the farthest distance from the WL and BL voltage sources (Fig.2.3). During the write operation, this leads to the smallest access voltage seen by the selected device. During the read operation, the number of cells which are connected to the reading path (i.e. BL_s) achieves its maximum. This leads to the largest leakage current, degrading the read signal.

b) Worst case data pattern

To determine the worst case data pattern, the cells inside the memory matrix are divided into four groups (Fig.2.4), namely the selected (SEL) cell, WL half-selected (WLHS) cells, BL half-selected (BLHS) cells and non-selected (NS) cells, according to voltage applied on their access WL_s and BL_s (the impact of wire resistance is ignored in the first order approximation).

Worst case data pattern for the write operation The worst case array pattern is that all the memory cells are put in the LRS (except for the selected one which depends on whether the SET or RESET operation is applied). This data pattern results in the highest leakage currents. On the selected WL and BL, this results in the largest

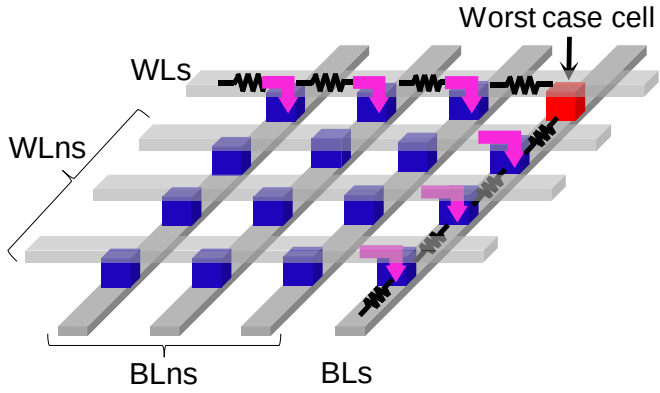


Figure 2.3: *Schematic of the worst selected cell location during memory operation. WL_s: the selected WL; WL_{ns}: the unselected WL_s; BL_s: the selected BL; BL_{ns}: the unselected BL_s.*

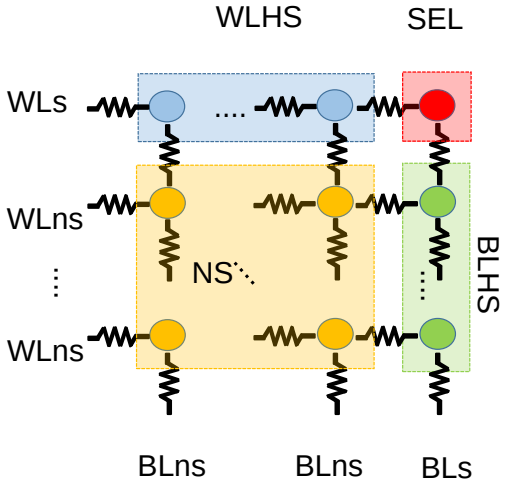


Figure 2.4: *In the worst case analysis, cross-point array elements are grouped into four categories according to the bias conditions.*

voltage drop. For the WLHS, BLHS and NS cells, this leads to the highest power consumption.

Table 2.1: The worst case data pattern under read and write operations

RESET	SET	Read logic '0'	Read logic '1'
ALL LRS	SEL: HRS	SEL: HRS	SEL: LRS
	WLHS: LRS	WLHS: LRS	WLHS: LRS
	BLHS: LRS	BLHS: LRS	BLHS: HRS
	NS: LRS	NS: LRS	NS: LRS

Worst case data pattern for the read operation Concerning the read operation, the total BL_s readout current has two contributors: the readout current of the selected cell and the leakage current of the BLHS cells. The worst data pattern corresponds to a minimum difference between the readout of the two different states of the selected cell. This situation occurs in the following case: (i) when reading a cell in LRS, and all the BLHS cells are in HRS and (ii) when reading a cell in HRS, with all the BLHS cells in the LRS. The RM can then be elaborated as, in eq.(2.4):

$$RM \cong \frac{[I_{SEL(LRS)} + n \cdot I_{BLHS(HRS)}] - [I_{SEL(HRS)} + n \cdot I_{BLHS(LRS)}]}{I_{ref}} \cdot 100[\%]$$
$$= \frac{\Delta I_{SEL(LRS)} - n \cdot [I_{BLHS(LRS)} - I_{BLHS(HRS)}]}{I_{ref}} \cdot 100[\%] \quad (2.4)$$

where n is the number of BLHS cells. This maximizes the RM degradation caused by the leakage from the BLHS cells, as emphasized by the term n·[$I_{BLHS(LRS)}$-$I_{BLHS(HRS)}$]. At the same time, if the WLHS and NS cells are in the LRS, this gives the highest power consumption during the read operation.

Table. 2.1 summarizes the worst case data patterns for both read and write operations.

2.2.4 Impact of the bias scheme

Different bias strategies can be employed for the cross-point memory arrays operation. For instance, ½ and ⅓-bias schemes are widely reported [113–116, 120–122].

a) ½-bias scheme

In a ½-bias condition, the unselected WL_s and BL_s are biased at the same ½V_{dd}, while the selected WL and BL are driven to V_{dd} and ground, respectively (Fig.2.5.a). This bias scheme minimizes the voltage drop on the NS cells. The power consumption, can thus be reduced since most of the cells in the array, i.e. $(n-1)^2$ cells are biased at

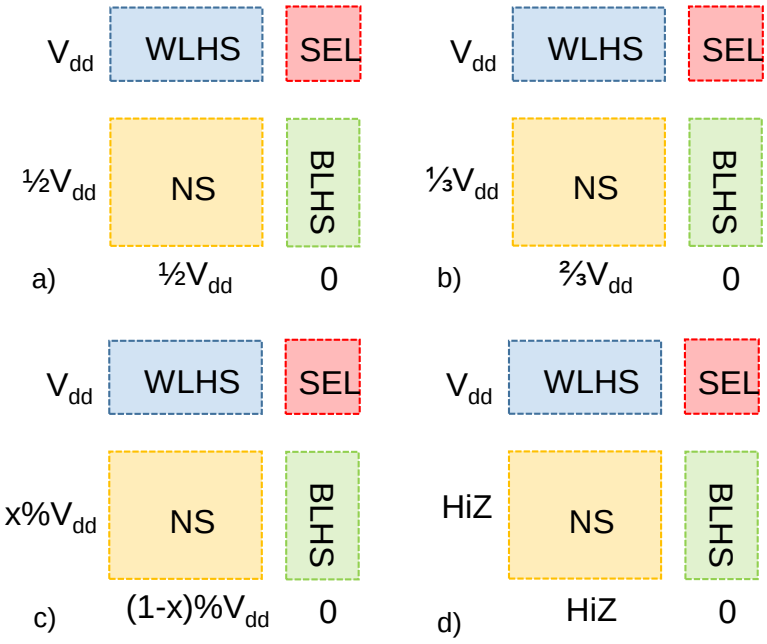


Figure 2.5: *Schematic of bias strategies for cross-point array (a) ½-bias. (b) ⅓-bias. (c) Optimal (partially) bias, x in between 1/3 and 1/2. (d) Floating bias.*

0V, where n refers to number of cells per WL or BL (assuming square shape array). However, the voltage drop on the WLHS and BLHS cells becomes large (e.g. ~½V_{dd}), as these cells are located in the critical path when accessing the selected device. The leakage currents through the half-selected cells strongly degrade both RM and WM.

b) ⅓-bias scheme

In an alternative ⅓-bias scheme, the unselected WL_s are biased at ⅓V_{dd} while the unselected BLs are biased at ⅔V_{dd} (Fig.2.5.b). This bias approach reduces leakage currents on the selected WL and BL, as the WLHS and BLHS cells see less voltage drop (i.e. ~⅓V_{dd}) as compared to ½-bias (i.e. ~½V_{dd}), which improves both RM and WM. However, the voltage drop over the NS cells increases and this may lead to significant increase of the total power consumption (note that the NS cells are biased at -⅓V_{dd}).

Table 2.2: Definition of various bias schemes for cross-point array

Bias Scheme	$\mathbf{V}_{WLS}$	$\mathbf{V}_{BLS}$	$\mathbf{V}_{WLNS}$	$\mathbf{V}_{BLNS}$
½ bias	V_{dd}	0	½V_{dd}	½V_{dd}
⅓ bias	V_{dd}	0	⅓V_{dd}	⅔V_{dd}
Optimized	V_{dd}	0	x% V_{dd}	(1-x)% V_{dd} [a]
Floating	V_{dd}	0	HiZ	HiZ

[a] ⅓$V_{dd} \leq x \leq$ ½V_{dd}.

c) Optimal bias

Neither ½ or ⅓-bias is likely to be optimal. An optimized bias scheme (Fig.2.5.c), optimizing the bias on the un-selected WL_s and BL_s, balancing array performance trade-offs in order to meet the RM, WM and power requirements is a more suitable bias condition, compared to the standard ½ and ⅓-bias schemes [115].

d) Floating bias

Another bias option for the cross-point memory is to leave the unselected WLs and BLs floating (Fig.2.5.d), i.e. the lines are terminated with high-impendence (HiZ). By reducing the number of voltage sources, the total memory power consumption decreases. However, in real circuit design, it is important to know the possible starting voltage range over the wires before executing the next operation to avoid cell disturbance due to the AC transient stress between two consecutive memory operations. Thus, when using a floating bias scheme, a conservative way is to wait for the floating lines until they reach their DC equilibrium. This may take a long time if the memory cells are highly resistive, since the RC constant of the floating nodes becomes very high. On the contrary, other bias schemes (i.e. ½, ⅓ and optimized) force and hold voltages on all lines to known states, therefore, they are preferable for practical circuits design.

A summary of various bias schemes reported for cross-point memory in the single-bit operation mode is listed in Table. 2.2.

2.3 Simulation framework for cross-point array analysis

To enable a quantitative analysis of cross-point memory array performance using arbitrary cell characteristics and memory size, a MATLAB-based simulation framework

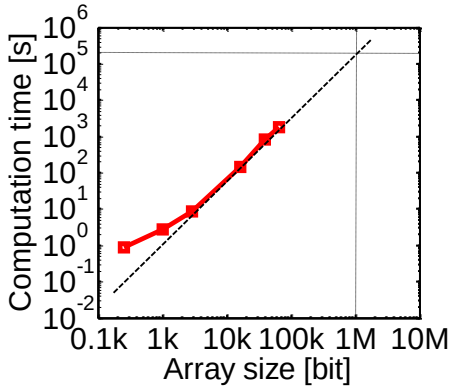


Figure 2.6: *Simulation time increases exponentially with increasing array size. Simulating 1Mbit array takes more than two days.*

is developed. In this part, we elaborate this simulation framework in detail.

2.3.1 SPICE circuit model

A 2D cross-point circuit netlist is developed in SPICE, based on the worst case analysis (i.e. worst case cell location and data pattern), assuming the single-bit operation mode. At this stage, selectors and memory cells either in the HRS or LRS are assumed identical, i.e. we use a variability-free approach. The circuit netlist contains the wire resistance, while the peripheral circuits and other parasitics (e.g. capacitances) are not considered. This circuit model enables DC SPICE analysis, which captures the main considerations for cross-point memory arrays due to the sneak current paths, i.e. access voltage drop, RM closure, power consumption, etc.

SPICE simulation provides accurate results. However, the computation time strongly depends on the complexity of the simulated circuits and simulating large size array becomes inefficient. Fig.2.6 extrapolates the computation time for 1Mbit array, which is estimated to be more than 56 hours. To improve the simulation efficiency, we introduce a method to evaluate the array performance in a computationally efficient, yet accurate way. A simplified netlist is developed by lumping small group of elements to an equivalent component. This allows for a fast estimation of the cross-point array performance while keeping acceptable accuracy.

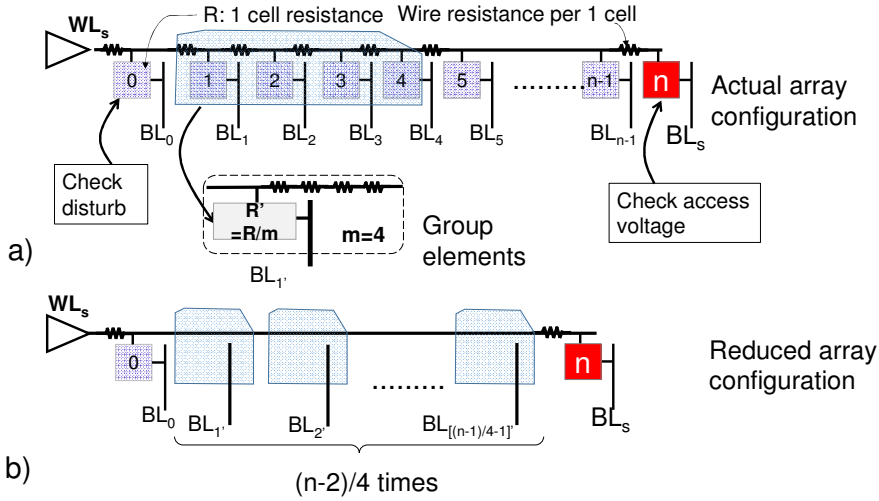


Figure 2.7: *(a) Actual array configuration for cells connected to the selected WL. (b) Reduced circuit configuration for WLHS cells and selected cell (rightmost) by lumping the nearby elements.*

When simulating large arrays, we are interested in the behavior of only a few cells, i.e. the selected device and the cells vulnerable to disturbance (close to voltage source), while taking into account the impact of the rest (Fig.2.7). Considering the worst case scenario, the first and the last cell along the selected WL are therefore of interest. For the rest of WLHS cells, even if the total voltage drop over the line can be large, however, the voltage difference between neighboring cells is small, so that these cells see almost the same potential. In the worst case data pattern (Table.2.1), assuming WLHS cells have the same characteristics, then we can merge 'm' elements together to a single component, with m times larger series line resistance (series lumping) and m times smaller cell resistance (parallel lumping). BL_1 to BL_m are reduced into a single node $BL_{1'}$, accordingly. This grouping method can be easily implemented using 'multiplier factor m' [123], which is supported by all SPICE simulators. Similar element-lumping approach is applied to the BLHS cells (Fig.2.8.a) and the NS cells (Fig.2.8.b). Note that for the non-selected (NS) cells, the line resistances in the 'm x m' block are lumped along both WLs and BLs directions. The merged line resistance along WL and BL can

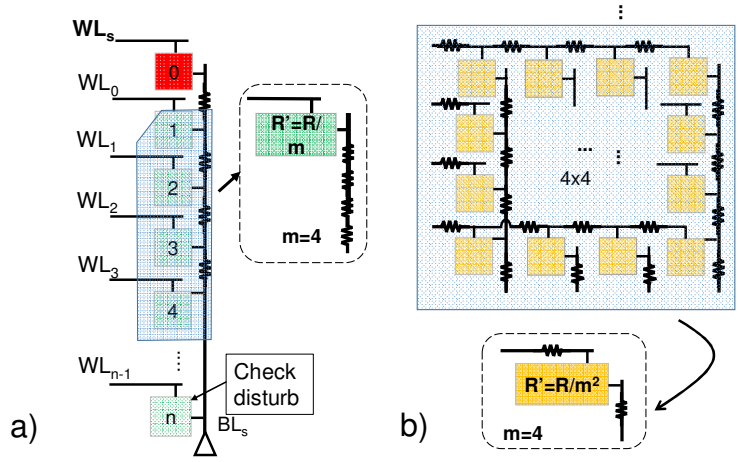


Figure 2.8: *Reduced circuit configuration for (a) the BLHS cells and (b) the NS cells .*

be calculated as follows:

$$R_{WL} = R_{line}/cell \cdot \frac{\#of\ cells\ lumped\ along\ WL}{\#of\ cells\ lumped\ along\ BL}$$
$$R_{BL} = R_{line}/cell \cdot \frac{\#of\ cells\ lumped\ along\ BL}{\#of\ cells\ lumped\ along\ WL} \tag{2.5}$$

In our case, the same lump factor m is used for both directions, therefore the lumped line resistance equals to the line resistance in the actual array configuration. The reduced circuit model is compared to actual array configuration (Fig.2.9). Several points need to be made for this simplified circuit model:

- A different multiplier factor m can be chosen for lumping, e.g. m=2,4,8,16, etc. It can happen that the amount of cells does not fit well for lumping. For instance, assuming 1Mbit (1024x1024) array and m equals to 4, (1024-2)/4 =255.5 which cannot be divided evenly. We can take two cells $_{(\#)}$ off from lump and treat them individually in the netlist, e.g. 2+255*4+2$_{(\#)}$. However, this approach is not flexible. To have an integer number of lumped cells, the array size is slightly adjusted to what fits more easily. For instance, assuming an array of 1026x1026, which can fit any multiplier factors 2^n, n=1,2, etc, with only 2 cells left out of the lumped circuit.
- The selector and resistive switching element (RSE) either in the LRS or HRS are identical from cell to cell in the matrix, i.e. a variability free approach is assumed unless otherwise mentioned.

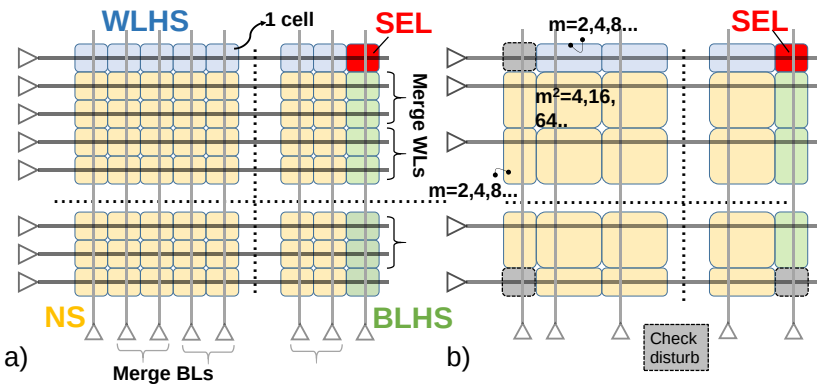


Figure 2.9: *a) Actual full cross-point array configuration. b) Reduced circuit model.*

- The worst case analysis is assumed as default, i.e. worst case data pattern, cell location.

SPICE simulation needs the input of device models. We use verilog-A lookup table model to describe the cell behavior for both selector element and RSE. The device Current-Voltage (I-V) characteristics can be either extracted from experimental results or predicted by a parametrized template. The approach taken to describe the device characteristics will be discussed individually in each chapter, since the models are selected in relation to the purpose of the simulation.

2.3.2 The simulation framework

The simulations are performed by using two software packages: MATLAB and Spectre. The former acts as a control program to manage the simulation flow, while the latter is a commercial simulator for SPICE circuit analysis.

(Fig.2.10) depicts the schematic of the simulation flow, which can be summarized as follows:

- At first, the 1S1R full cell behavior is constructed by combining serially connected selector and RSE. The generated full cell characteristic is then written using the Verilog-A lookup table model. The full cell parameters, such as the set, reset and read voltages are extracted from the simulated full cell characteristics.
- The 1S1R Verilog-A model together with other array configuration parameters, e.g. cross-point array size, wire resistance, (worst case) data pattern, lumping

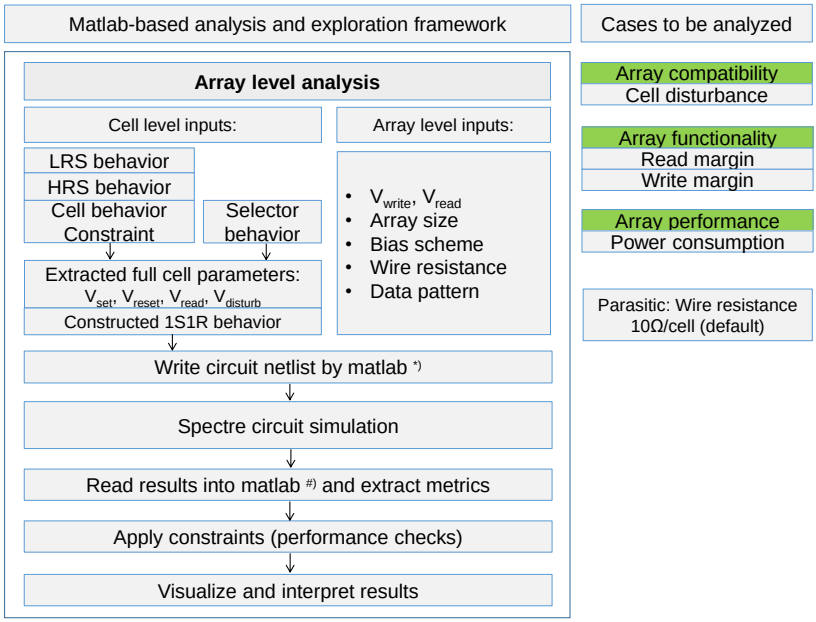


Figure 2.10: *Simulation flow for 1S1R array level performance evaluation. ∗) The lumped circuit netlist is created by using an in-house developed MATLAB toolbox: mat2spice [124]. #) The Spectre simulation output results are read into MATLAB by using an in-house developed MATLAB toolbox: Signal Storage [125].*

factor, bias scheme, read/write voltage (i.e. determined by the extracted full cell parameters in the previous step) are utilized as inputs to write the circuit netlist.

- The circuit simulation is executed by calling Spectre.
- The output results are read into MATLAB for visualization and interpretation. The array operation FOM's, i.e. the RM, WM and read/write power consumption are checked.

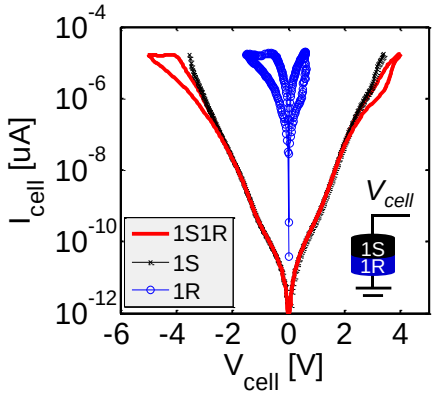


Figure 2.11: *Constructed 1S1R full cell behavior (line) by combing the experimental results of selector (cross) and RSE (circle), cell size: 40x40nm.*

2.3.3 Model Validation

A sanity check of the simulation accuracy is to change the multiplier factor 'm' for the simplified circuit model and compare the results. As an example, the experimental I-V characteristics of Ultra-Thin-HfOx (UTO) resistive memory [126] and Metal-Silicon-Metal (MSM) selector [127] are digitized and used as inputs for the simulation. The individual cell behavior and the combined full cell characteristics are shown in Fig.2.11. The full cell set voltage is extracted around +4V, and the read voltage is set at +3.3V. We monitor the access voltage drop on the selected cell during the set operation, the RM and power consumption as a function of array size, and compare the results under different lumping strategies (Fig.2.12).

For instance, '8x8' refers to the effective array size, meaning the multiplier factor m=128 for 1026x1026 array, m=64 for 514x514, m=32 for 258x258, etc. While '16x16' corresponds to m=64 for 1026x1026, and so forth. We compare the results between the lumped circuit model and matrix without simplification, concluding that the difference is negligible. This suggests that the lumped-element approach provides an effective method to keep the computation time low, without sacrificing the simulation accuracy.

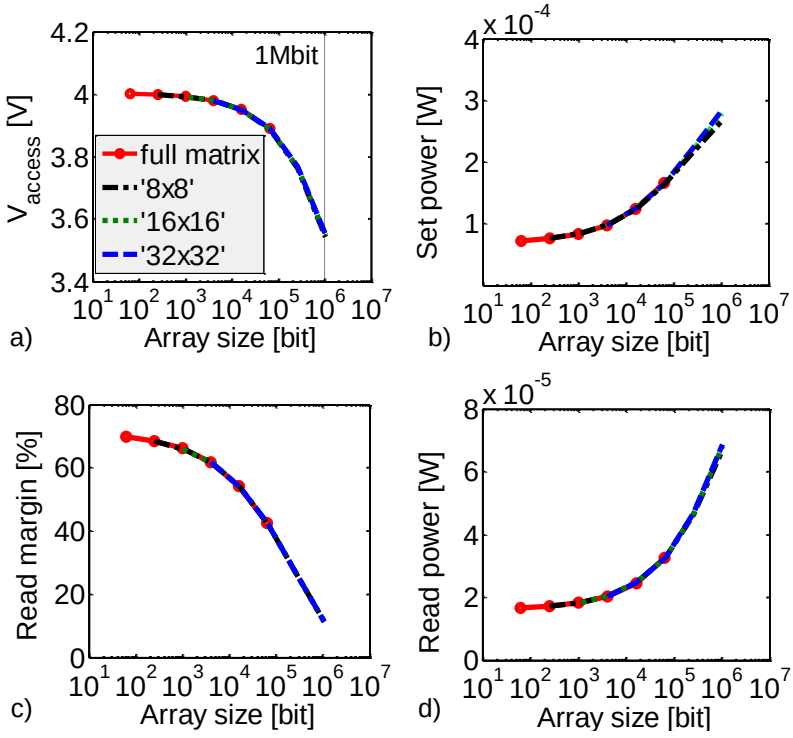


Figure 2.12: *Simulated (a) access voltage drop (b) SET power (c) read margin (d) read power based on the reduced circuit model using various lumping approaches. The simulated array is under ½-bias scheme.*

2.4 Conclusion

In this chapter, we discussed the fundamentals of the cross-point memory array, including the strategies for read and write operations, the figures-of-merit for assessing the array performance, the worst case patterns and the trade-offs among various bias schemes. An efficient SPICE circuit simulation methodology is developed in order to quantify the quantify the cross-point array behavior. Using a lumping method, this approach enables a good compromise between computation time and simulation accuracy, offering an efficient and accurate way for simulating large arrays. Finally, a MATLAB-based analysis framework is presented. This tool stands at the basis of the research work reported in this Ph.D. thesis.

Chapter 3

Extraction of ideal behavior for selector and resistive memory element

3.1 Introduction

In this chapter, a comprehensive circuit-level simulation is performed to investigate the impact of 1S and 1R characteristics on the overall cross-point array performance. We derive the cell requirements using a top-down approach, based on the simulation framework described in Chapter 2. The requirements that a 1S, 1R cell need to fulfill are extracted, considering sets of figures-of-merits describing the array functionality and performance, under various array bias conditions. This circuit-to-device interaction analysis enables for evaluating various selector and resistive switching element (RSE) concepts. Furthermore, it provides engineering guidelines for the 1S1R cell implementation.

This chapter is organized as follows: in section 3.2, we first investigate the impact of the selector characteristics on the 1S1R performance. Two types of selection devices, i.e. showing non-abrupt I-V characteristics and Threshold Switching (TS) selectors are evaluated. For a given RSE performance, the requirements for both selector candidates are extracted for a 1Mbit array, taking into account the read/write margin and power consumption constraints. Taking the extracted selector requirements as target, different selectors reported in literature are evaluated and the improvement directions are suggested. In section 3.3, we further investigate the impact of the resistive

switching element (RSE) characteristics, focusing on the low resistive state resistance R_{LRS} and high resistive state resistance R_{HRS}. For a given selector performance, we find that there is an optimal R_{HRS}/R_{LRS} ratio, which improves the overall performance of the read operation in the array. The final conclusion of this chapter is summarized in section 3.4.

3.2 Selector requirement extraction

In literature, the performance of the 1R-only cross-point array has been extensively investigated [113, 122, 128–134]. A limitation of the this analysis is that the selector element is not considered. With an increasing emphasis on the 1S1R cross-point array development and integration for high density memory applications, a systematic study for the selector element is needed. The main purpose of this work is to evaluate what kind of selector characteristics are required to guarantee an acceptable array performance.

3.2.1 Methodology

To derive the requirements for selector from the array perspective, a SPICE-based simulation framework (as detailed in section 2.3) is employed. Considering the fact that the 1S1R arrays target for high density memory applications, we fix the array size to 1Mbit in this study (using a default lump factor, m=8). The 1Mbit array size is chosen for comparison with 2D single level cell (SLC) NAND flash memory [135]. A single block of the NAND memory contains 64 pages with each page size equals to (2024+64) bytes. This translates to each block size at ~1Mbit.

In addition to the intrinsic properties (e.g. manufacturability, reliability, etc), selector suitability for 1S1R memory arrays depends on the characteristics of the RSE and the circuit parameters (e.g. bias scheme, array size) [50]. To limit the number of variables, we assume an ideal RSE with fixed behavior (known parameters) by default, while injecting the parameter variation only to the selector behavior and array bias scheme. Fig.3.1 depicts the simulation flow. The selector characteristics are modeled using a flexible parametrized template. By changing the model parameters, various characteristics can be generated. We scan a wide range of selector characteristics by varying the template parameters, and the array bias schemes. For each case, a set of figures-of-merits (i.e. read margin, write margin, read/write power consumption) of the array performance are calculated through the simulation flow. In the end, a relationship between input parameters (i.e. selector characteristics, bias schemes) and output results (i.e. array performance) can be established, as shown in eq.(3.1), where P_1,P_2, etc refer

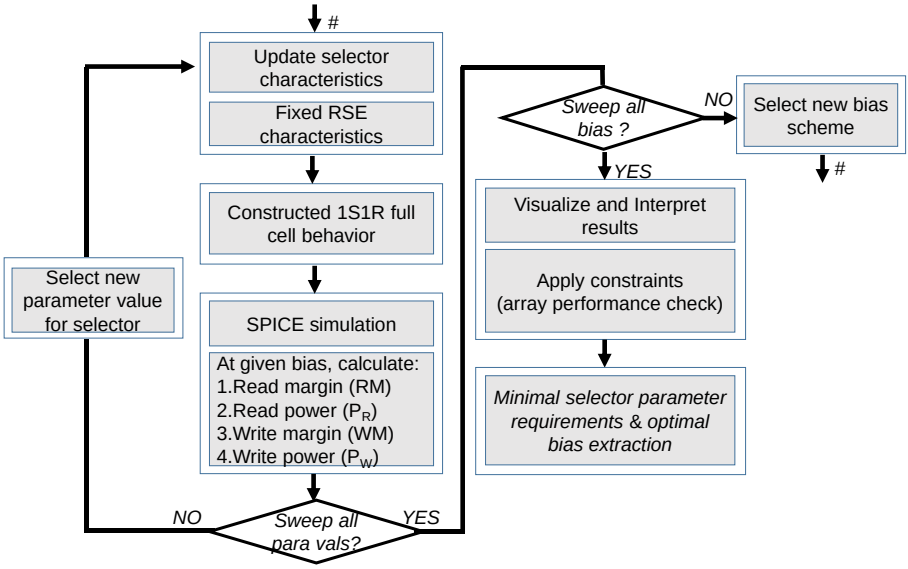


Figure 3.1: *The simulation flow chart for selector requirements extraction.*

to the different selector parameters.

$$FOM_{array} = f_{selector}(P_1, P_2, ..) \cdot f_{array}(bias) \tag{3.1}$$

For an array to be functional, it must provide sufficient read margin and write margin. Furthermore, the total read and write power consumption are also important indicator for the array performance. Therefore, these four parameters are employed as figures-of-merit, the definition and the minimum requirements are listed in TABLE.3.1. A 25% difference in the readout current is defined as the minimal criterion for distinguishing the selected cell state. During the write operation, the maximum voltage drop on the selected interconnect (WL_s and BL_s) is defined as less than 10% of the applied voltage for the selected cell. The constraints for the power consumption are defined as follows: below 1mW for the write operation and below 10μW for the read operation. If we assume the access time of 100ns for both read and write, these limits lead to an energy per accessed bit of 1pJ/bit for the read and 100pJ/bit for the write operations, respectively. As a reference, in NAND Flash, the lowest energy values reported for single-level cell is 42pJ/bit for read, 410pJ/bit for program [136] (data are from different products, and the values include the energy consumption of the peripheral circuits), which shows that RRAM may be competitive from an energy consumption point of view. Under the applied the RM, WM and power consumption constraints, the selector parameter requirements and the optimal bias condition (i.e. which allow for the widest selector parameters region) can be determined accordingly.

Table 3.1: FOM and the minimum performance requirements for 1Mbit Array

Figures-of-merit	Definition	Min.requirement
read margin (RM)	ΔI_{BLS}/I_{ref} [a]	$\geq 25\%$
write margin (WM)	V_{access}/V_{dd}	$\geq 90\%$
read power (P_R)	total power consumed from voltage sources	$\leq$10μW per accessed bit
write power (P_W)	total power consumed from voltage sources	$\leq$10mW per accessed bit

[a] I_{ref}=I_{BLS}, when the selected cell is in LRS.

Finally, it should be noted that we assumed a variability-free approach, which means that the modeled selector and RSE behavior, either in LRS or HRS are identical from all cells in the cross-point array.

3.2.2 Device model

In this part, we introduce an approach to model the resistive switching element and the selector element, respectively.

3.2.2.1 The RSE model (1R)

A "forming process" is commonly required to initialize the cell into the switching mode by applying a high voltage. However, this process increases the complexity of the circuit design and increases the risk of selector damage in the 1S1R cell, as most of the voltage applied during the forming transfers from the RSE to the selector immediately after forming takes place. A forming-free RSE [126, 137, 138] , of which the very first switching (forming) process is not differentiated from the subsequent set operations, is an ideal RSE for an 1S1R implementation. In this work, we did not specifically model the forming process. Instead, only the switching characteristics are considered.

The RSE is described using the parameterized template with a fixed behavior (Fig.3.2). The RSE has two distinct non-volatile states, the LRS and HRS. For simplicity, both states are assumed to be Ohmic, where R_{HRS} is fixed at 500kΩ and R_{LRS} equals to 50kΩ, resulting in an on/off ratio of 10, which reflects the typical resistance ratio (median) for HfO_x based RSE [17, 126]. For an ideal RSE, low switching current is required, mainly due to two reasons. From the selector perspective, this relaxes the drive current requirement, since the selector must provide enough current to enable the RSE switching in the cell. Next to it, low switching current reduces the IR voltage drop on the interconnects, power consumption and further improves the circuit reliability.

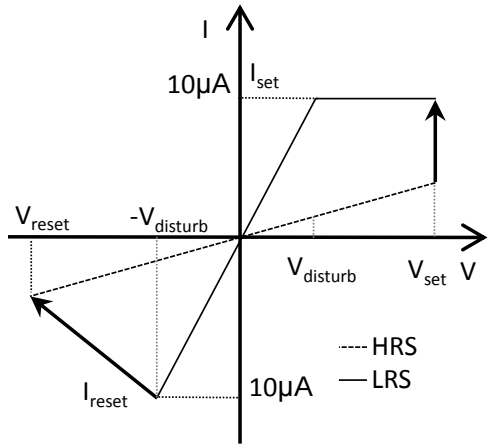


Figure 3.2: *Generic model for 1R element with bipolar switching characteristics.*

For instance, potential electro-migration (EM) issues for the scaled interconnects can be alleviated. However, low current usually leads to RSE performance degradation in terms of increased variability and reliability [59–61]. Considering the trade-offs in practice, this implies that switching current of around 10µA is reasonable for an ideal RSE. Furthermore, the resistive switching can be considered as self-compliant, which means no extra compliance needs to be applied to limit the switching current. For filamentary RSE, this can be achieved by using an external transistor. In generally, a current-compliant RSE (i.e. either being self-complaint or limited by external transistor) is required due to the fact that a selector can hardly act as an ideal current compliance element, since its resistance decreases with increasing the bias. The modeled RSE is assumed to have symmetrical set and reset voltages of $\pm$1.5V, which is representative a typical HfO_x based RSE [17, 126]. Moreover, a low operation voltage is beneficial for the circuit design, as it, e.g., simplifies the charge pumping circuitry. The disturb voltage determines the maximum voltage drop on the RSE, beyond which the cell state may change unintentionally. At this stage, we fix the disturb voltage value of $|\pm$0.5V|, i.e. +0.5V: HRS to LRS, -0.5V: LRS to HRS disturbance.

All default model parameters are listed in TABLE.3.2. In summary, this parametrized model captures the key RSE features, considering the characteristics of an ideal RSE.

3.2.2.2 The selector model (1S)

So far, many selector concepts have been reported in literature where we have introduced some of them in Chapter 1. Instead of modeling the selector characteristics

Table 3.2: Default RSE model parameters

Parameter	Symbol	Default value
Switching current	I_{switch}	10μA
SET voltage	V_{SET}	+1.5V
RESET voltage	V_{RESET}	-1.5V
HRS resistance	R_{HRS}	500kΩ
LRS resistance	R_{LRS}	50kΩ
Disturb voltage	$V_{disturb}$	0.5V

using different analytical equations according to their underlying physical mechanisms, we simply group them into two categories according their behavior. In the following, we will refer to the first category as to type-I selectors, in contrast to type-II selectors, for the second category. For selectors in each group, a 'universal' model is employed to describe the cell characteristics.

- **Type-I selectors** generate non-linear I-V characteristics, where the current gradually changes with the applied voltage without any abrupt I-V transition. This non-linear behavior can be generated by electron tunneling [91, 94, 139], Schottky emission [87, 89], punchthrough NPN [81] and Mixed-Ionic Electron Conduction (MIEC) [112], etc.
- **Type-II selectors** show I-V behavior characterized by an abrupt increase of the current, for voltage-controlled sweeps. This corresponds to S-type voltage snapback, with a negative differential resistance (NDR) between a threshold voltage (V_{th}) and a hold voltage (V_{hold}), for current controlled sweeps. In voltage-controlled sweeps, the NDR region is unstable, i.e. an abrupt and reversible transition occurs to either a high resistive state (off-state) or to a conductive state (on-state). Typical examples includes Chalcogenide based Ovonic Threshold Switching (OTS) [105], Metal-Insulator Transition (MIT) [62, 140] Field Assisted Superlinear Threshold (FAST) [108] and Threshold Vacuum Switching (TVS) [141].

a) Type-I selector model The type-I selector characteristics are modeled using a flexible template Fig.3.3.(a). This model generates non-linear I-V characteristics through the following exponential equation,

$$I(V) = \frac{V}{R_0} \cdot e^{\frac{V - V_{op}}{\alpha}} \tag{3.2}$$

where V_{op} determines the operating voltage range of the selector, i.e. the voltage at which the maximum drive current $I_{drive} = V_{op}/R_0$ is achieved and R_0 is the selector

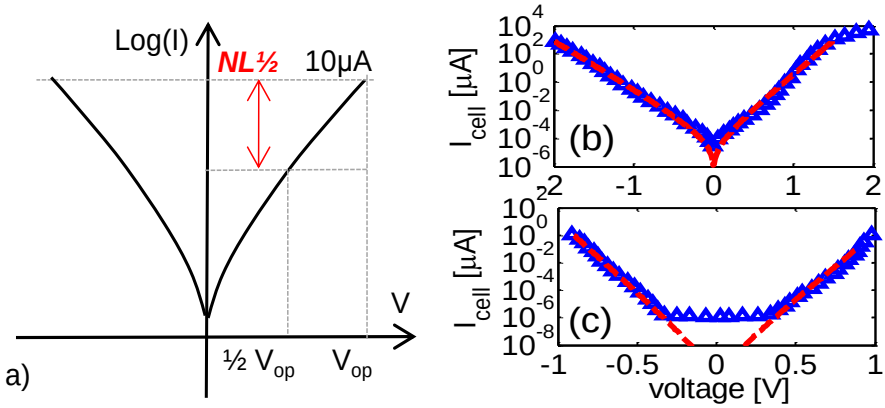


Figure 3.3: *(a) Modeled symmetrical type-I selector behavior. b) Flexible template fits well with reported selector (b) Varistor [94] and (c) MIEC [112]. Dash line: model prediction. Symbol: experimental data. The flat I-V in (c) is due to resolution of the measurement system.*

large signal resistance at V_{op}. The drive current I_{drive} for the selector is fixed by the peak switching current of the RSE, e.g. 10μA, (Fig.3.2). Although there are many ways to express the nonlinearity of a selector, here we use the half-bias definition, where the half-bias nonlinearity (NL½) is defined as the ratio between the current at the operating voltage (e.g. 10μA, as a reference) and the current flowing through the selector, when it is biased at ½V_{op}. The selector nonlinearity is determined by the coefficient $\alpha \propto 1/Ln(NL_{1/2})$.

This parameterized model is flexible in that it can fit very well with various reported selector characteristics Fig.3.3.(b-c). By sweeping the independent model parameters, i.e. V_{op} and NL½, a family of non-linear I-V characteristics can be generated, which covers a wide range of selector, independent of the underlying conduction mechanisms.

b) Type-II selector model

Fig.3.4 represents a typical type-II behavior showing an S-shape transition during the current-controlled I-V sweeps. A snapback transition from the off-state to the on-state is triggered by applying a voltage exceeding a critical value, called the threshold voltage (V_{th}). The on-state maintains for as long as the current flowing through the cell above a certain limit, called the holding current (I_{hold}). When the current through the element is reduced below this limit, the on-state cannot be hold anymore and the cell goes back to the initial off-state immediately. This S-shape transition is unstable and can be captured only in the current-controlled I-V sweeps. This corresponds to the I-V

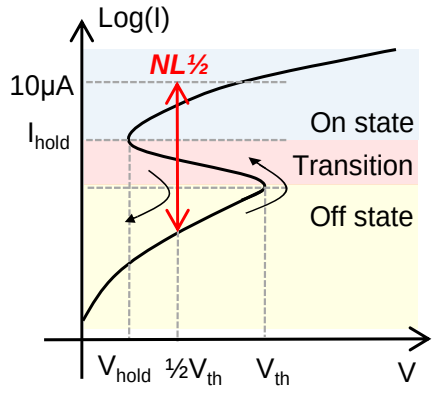


Figure 3.4: *Schematic of Type-II selector behavior characterized in current-controlled I-V sweeps.*

behavior characterized for voltage-controlled sweeps, as depicted in Fig.3.5. A simple method to model the type-II selector behaviors is to consider only the on-state and off-state characteristics. Indeed, in the practical memory operation (i.e. controlled by the voltage), type-II selectors will be biased either in the off-state (e.g. to cut off the leakage current) when the 1S1R full cell is partially-selected or unselected, or in the on-state (e.g. to be fully turned on), to allow sufficient access voltage drop on the target memory element (e.g. selected for read/write). From this point of view, the steady-state type-II selector characteristics are more important than that of the transition, which affects the overall memory performance.

The selector's volatile on and off-states are modeled in a separate way. It is reported that the off-current in Chalcogenide based threshold switching material typically obeys the Poole-Frenkel (P-F) conduction mechanism [99, 100, 105]. Therefore, we model the off-state I-V using a simplified P-F equation as follows,

$$I(V) = \alpha \cdot V \cdot e^{\beta\sqrt{V}} \tag{3.3}$$

The reference current is fixed at 10μA. The NL½ for TS selector is defined as the ratio between the reference and current when selector is biased at $½V_{th}$. This non-linearity definition is in line with that of the type-I selector. α and β are the fitting parameters.

The linear I-V characteristics are observed in the on-state of various threshold switching materials. For this reason, we simply describe the on-state by the Ohmic resistance (R_S). The on-state current is then given by,

$$I(V) = V/R_S \tag{3.4}$$

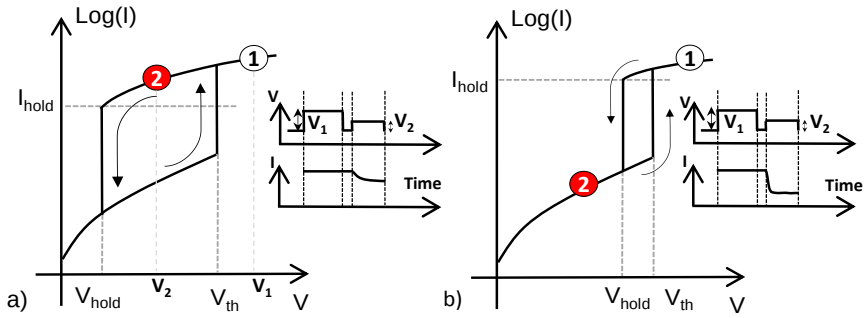


Figure 3.5: *Schematic of selector behavior in voltage-controlled double sweeps. Selector with (a) low holding current and low holding voltage. (b) high holding current and high holding voltage.*

The parameter I_{hold} and V_{hold} that determine at which point the selector switches back to its off state can be important if we consider consecutive memory operations on the same 1S1R cell, e.g. to be selected for read or write first, and then to be partially biased as unselected (or half-selected). The 1^{st} operation requires the selector to be fully open, e.g. a large voltage 'V1' is applied (Fig.3.5.a). While during the 2^{nd} operation, a low voltage drop (e.g. 'V2') on the selector is required, aiming to keep it in the off-state for reducing the full cell leakage current. However, in case the selector is not fast enough (e.g. it remains in the on-state before executing the next operation), even though a low bias is applied during the 2^{nd} operation, the selector may still stay in the on-state (Fig.3.5.a,inset) when the holding voltage is smaller than 'V2'. In this case, a large holding current (voltage) is preferred (Fig.3.5.b).

Considering a fast type-II selector, I_{hold} and V_{hold} are no longer important, i.e. selector switches to off-state during the interval between pulse voltage 'V1' and 'V2'. Therefore, to simplify the following analysis, we do not specifically take these two parameters into account in the type-II selector template, and only consider the steady-state of type-II selector.

To conclude, the three parameters: 1) V_{th}; 2) NL½; and 3) R_S are employed to describe the general type-II selector characteristics, of which can be varied independently (free parameters).

Table 3.3: Type-I selector template parameters

Selector	**A**	**B**	**C**
I_{drive}(μA)	10	10	10
Operating voltage $\|\pm V_{op}\|$ (V)	3	1	1
Half-bias NL½	10^4	10^4	10^2

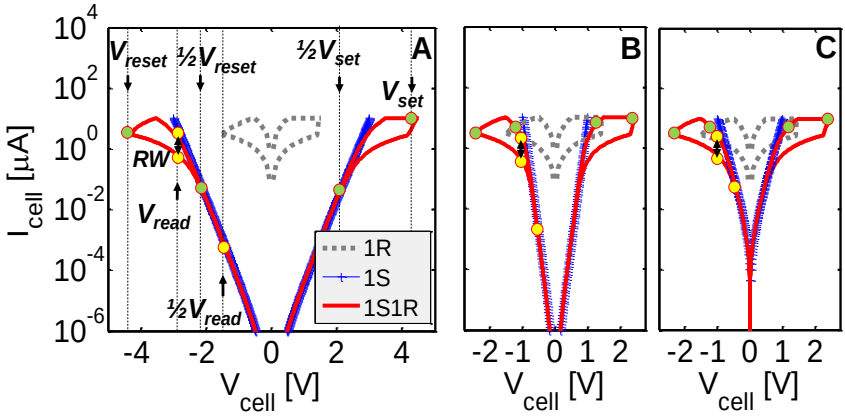


Figure 3.6: *Simulated 1S1R full cell characteristics (red solid) by combining the I-V of the default RSE (dash) and 1S selector template (cross). Selector parameter: (A) V_{op} =3V, NL½ =10^4 (B) V_{op} = 1V, NL½ = 10^4 (C) V_{op}=1V, NL½ =10^2. The dots indicate the points used to extract the full cell performance factors in TABLE.3.4.*

3.2.3 1S1R cell level analysis

3.2.3.1 Type-I selector

The DC I-V characteristics of the full 1S1R cell are constructed by combining the default RSE with the parameterized type-I selector I-V characteristics. Several 1S1R performance trade-offs can be determined by analyzing the full cell behavior using selectors with different operating voltages V_{op} and NL½ at specific cell operation conditions. The input selector parameters under evaluation are listed in TABLE.3.3. Fig.3.6 shows the simulated 1S1R full cell characteristics by combining the RSE with the selector templates, namely A, B and C.

In the read operation, the maximum read voltage for the full cell is limited by the disturb voltage for the RSE, e.g. $|\pm 0.5V|$ in our case. In reality, a higher voltage always cause earlier and larger onset of the resistance change, thus a consecutive read

Table 3.4: Extracted 1S1R full cell performance matrix

1S1R		**A**	**B**	**C**
Read	V_{read}(V)	-2.8	-1.1	-0.9
	Read window (RW)	3.4	5.3	3.2
	I_{LRS}(½V_{read})(nA)	0.6	1.0	71.1
	NL½(read): I_{LRS}(V_{read})/I_{LRS}(½V_{read})	3294	1977	28
Write	V_{reset}(V)	-4.5	-2.5	-2.5
	V_{set}(V)	4.5	2.5	2.5
	I_{LRS}(½V_{reset})(μA)	0.1	5.6	6.1
	I_{LRS}(½V_{set})(μA)	0.1	5.6	6.1
	NL½(write): 10μA/I_{LRS}(½V_{set}or½V_{reset})	96.3	1.8	1.6

operation close to the disturb voltage may lead to fast state change. For this reason, a lower read voltage is assumed, i.e.-0.1V, as the read voltage drop over the RSE at read condition. Due to the symmetrical I-V characteristics for both 1S and 1R elements, it does not cause much difference between positive and negative polarity for the read operation. The read voltage (V_{read}) applied on the 1S1R full cell is defined as the voltage which will cause a voltage drop of -0.1V on the 1R element in the LRS. The key performance indicators of the 1S1R full cell, i.e. the read voltage (V_{read}); the read window (RW), which define the on/off current ratio (I_{LRS}/I_{HRS}) at readout voltage (V_{read}); NL½ (read), which is the ratio between the LRS current at V_{read} and ½V_{read}, are extracted in TABLE.3.4.

It should be noted that the full cell RW decreases, compared to that of 1R-only case (RW=10). The reason is that the selector shows a relatively large resistance compared to that of the RSE at the applied V_{read}. Therefore, the voltage drop on the 1R in the LRS is smaller compared to HRS, resulting in a degraded RW. Reducing the V_{op} of selector maximizes the full cell RW and reduces the read voltage, since a low V_{op} at fixed current drive is associated with a lower selector resistance at readout condition. Selector with large NL½ improves the full cell NL½ , as the leakage current at half read bias strongly reduces. However, the operating voltage determines how much nonlinearity can be transferred to the full cell. To this end, large V_{op} is preferred (e.g. selector A) because it would further decrease leakages during the read operation.

In summary, a higher V_{op} increases the 1S1R cell nonlinearity, but decreases the RW and increases the read voltage.

Concerning the write operation, due to symmetrical characteristics for both 1S and 1R elements, full cell performance is similar for the reset and set operations (TABLE.3.4). The selector with low V_{op} reduces full cell voltage required for the write operation, which is preferred. However, the non-linearity of the selector with small V_{op} diminishes when considering the whole 1S1R cell, even if the selector itself has high NL½.

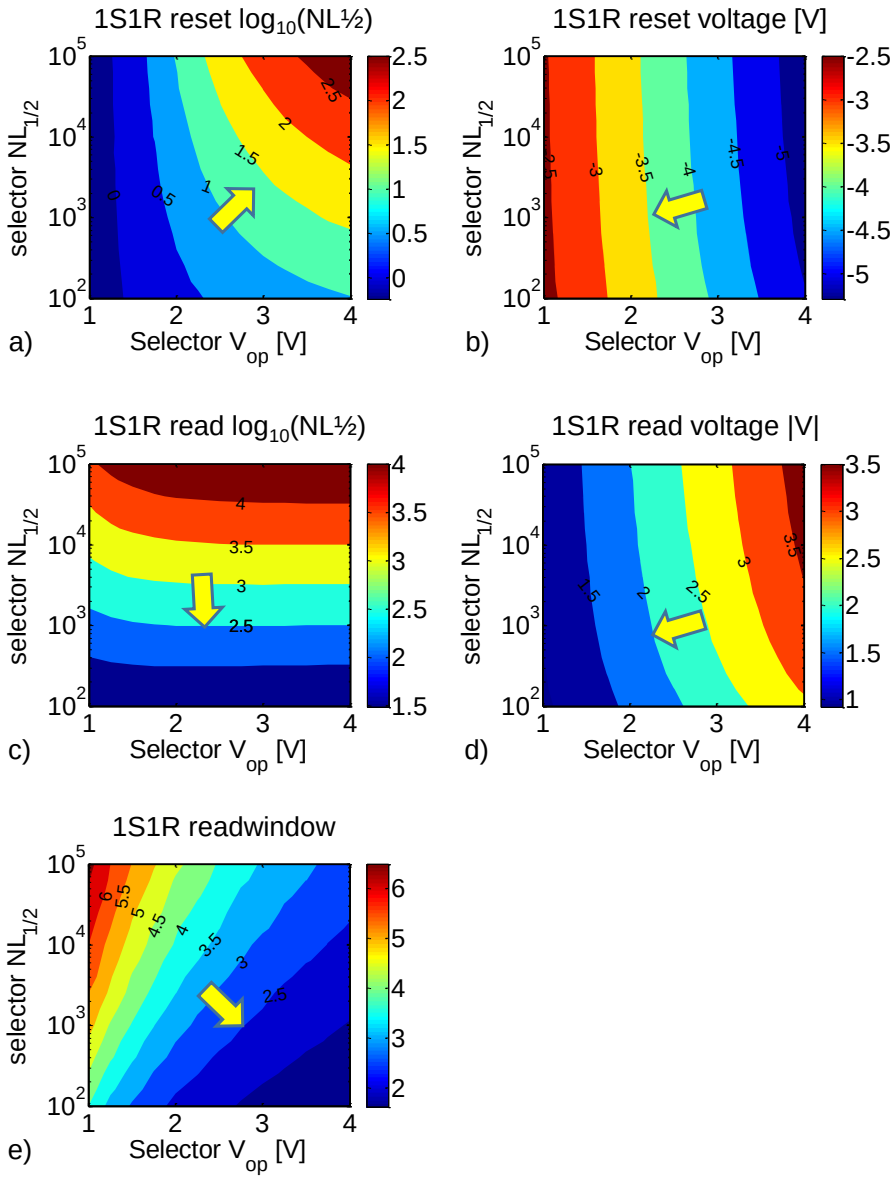


Figure 3.7: *Contour plots for the full cell characteristics (scales on the color bar) (a) reset NL½ (b) reset voltage (c) read NL½ (d) read voltage (e) RW as function of selector parameters: selector NL½ (x-axis) and Selector operation voltage (y-axis). The arrow shows the best improvement direction for reaching the full cell performance targets. The different arrow directions evidence the trade-offs for the 1S1R cell configuration.*

The main reason is that the selector resistance is small compared to that of 1R element in a large part of the relevant voltage range. As a consequence, the voltage applied to the cell would be mainly transferred to the RSE. The non-linearity of the full cell is given by the non-linearity of the RSE, which is linear in the LRS. Hence, a low selector V_{op} allows for a lower program voltage for the 1S1R full cell, but at the cost of reduced non-linearity.

To get a full picture of how selector characteristics impact the full cell performance, selector parameters NL½ and V_{op} are varied over a wide range and resulting 1S1R characteristics are plotted in Fig.3.7.

The arrow shows the 1S1R performance improvement direction and the selector characteristics requirements in order to achieve that. The different orientation for each arrow indicates trade-offs for fulfilling a low voltage operation, large RW, high non-linearity 1S1R cell characteristics for both read and write operations.

3.2.3.2 Type-II selector

The selector showing threshold switching behavior causes other 1S1R cell issue, i.e. read disturb, which is due to its rapid transition from the highly resistive off-state to the low resistive on-state.

During the read operation, in order to open-up the full 1S1R cell RW, the type-II selector needs to switch into its on-state when V_{read} is applied. The V_{read} should be large enough, so as to cause a voltage drop of V_{th} on the selector to make the transition happen. After that, due to the negative differential resistance (NDR), the resistance of the selector dramatically decreases. If the selector on-state resistance R_S is much smaller than the resistance of the RSE, most of the voltage on the selector will immediately transfer to the RSE. This causes read disturbance of the RSE when the transferred voltage is larger than its disturb limit (e.g. 0.5V).

A simple procedure is employed to check whether or not read disturb occurs in the 1S1R cell for a given type-II selector performance. We firstly serially combine the I-V characteristics of the $HRS_{(1R)}$ and the $off\text{-}state_{(1S)}$. From that, the voltage (V_{th_1S1R}) that needs to be applied on the full cell, which causes a voltage drop of V_{th} on the selector can be extracted. The applied read voltage should be large enough to turn on the selector. We arbitrary define the full cell V_{read} as ($V_{th\_1S1R+20mV}$). As the next step, we calculate the voltage distribution over the RSE and R_S when the read voltage ($V_{th\_1S1R+20mV}$) is applied. If the voltage drop over the RSE exceeds the predefined disturb limit (e.g. 0.5V), which means that disturb occurs. Thus, the type-II selector is not suitable for the default RSE.

We sweep selector parameters V_{th} and R_S over a wide range, while keeping NL½

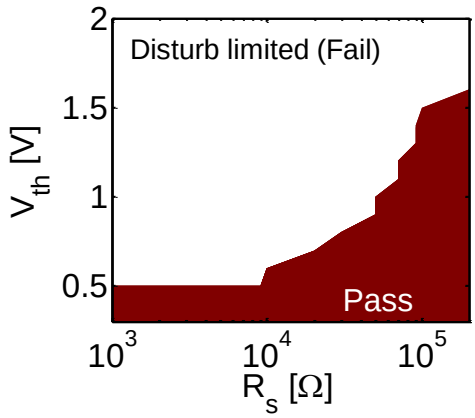


Figure 3.8: *Extracted selector parameters (V_{th} and R_S) design margin under read disturb constraint. Voltage drop on the 1R exceeds 0.5V (Fail), below or equal to 0.5V (Pass). Selector non-linearity is fixed at NL½=10^4.*

constant. For each generated type-II selector behavior, 1S1R cell read disturbance is checked. As a result, the improper selector parameter design region can be screened out (Fig.3.8). We find that the read disturb is strongly affected by V_{th} and R_S, while it is almost independent of NL½ variation. In Fig.3.8, when R_S is small, most of the applied read voltage will transfer to the RSE since the selector on-state resistance is much lower than that of RSE. In this case, reducing V_{th} is essential, as it decreases the full cell V_{read}. The maximum voltage (i.e. V_{read}) that can be transferred to the RSE is limited (Fig.3.8, left part). With increasing V_{th}, larger R_S is required to protect the RSE. Since the amount of voltage transferred to the RSE depends on the ratio between the R_{HRS} and R_S. With a large R_S, most of the voltage drop over in the selector element after selector transition takes place (Fig.3.8, right part). Note that, $|0.1V|$ is used as a boundary to determine the full cell read voltage for the type-I selector. However, when the same boundary is assumed, this results in a limited parameter design margin for the type-II selector (not shown). Therefore, we increase this boundary, e.g. up to 0.5V, in order to improve the selector parameter design range. As we mentioned before, however, cumulative stress from high read voltage over the RSE accelerates the unintentional resistance change (e.g. disturb occurs earlier). This indicates that the selector parameter design margin trades off with the disturb immunity in the 1S1R cell configuration using the type-II selector.

Besides the read disturb issue, 1S1R performance has to fulfill the requirements derived from the circuit level, which means low operating voltage, high non-linearity and large read window are desired. However, several performance trade-offs have been observed

when we combine the default RSE with various type-II selector behaviors.

Table 3.5: Type-II selector template parameters

Selector	**A**	**B**
Threshold voltage $\|V_{th}\|$(V)	0.4	1
Half-bias NL½	10^4	10^4
On-state R_s(kΩ)	1	100

Table 3.6: Extracted 1S1R full cell performance matrix

1S1R		**A**	**B**
Read	V_{read}(V)	0.42	1.02
	Read window (RW)	10	4
	I_{LRS}(½V_{read})(nA)	1.2	1.0
	NL½(read): I_{LRS}(V_{read})/I_{LRS}(½V_{read})	6560	6832
Write	V_{reset}(V)	-1.5	-1.8
	V_{set}(V)	1.5	1.8
	I_{LRS}(½V_{reset})(nA)	8530	24
	I_{LRS}(½V_{set})(nA)	10^5	24
	NL½(write): 10μA/I_{LRS}(½V_{set}or ½V_{reset})	1	424

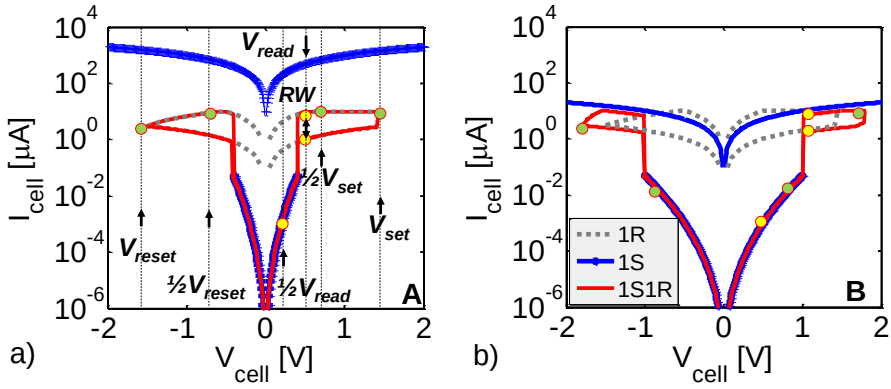


Figure 3.9: *Simulated 1S1R full cell characteristics (red solid) by combing the I-V of the default RSE (dash) and 1S selector template (cross). Selector parameter: (a) V_{th}=0.4V, NL½=10^4, R_S=1kΩ. (b) V_{th}=1V, NL½ =10^4, R_S=100kΩ. The dots indicate the extracted full cell performance indicators.*

As an illustration, two selector characteristics are chosen for comparison (TABLE.3.5). The parameter values are picked up from 'Pass' region in Fig.3.8, to avoid the occurrence of the read disturb. The constructed 1S1R characteristics are plotted in Fig.3.9 and the extracted full cell performance indicators are listed in TABLE.3.6.

For selector A, the full cell RW remains un-degraded compared to the 1R-only configuration (RW=10), thanks to the low on-state Rs (1S), e.g. close to 0V drop over the selector. As a result, the RSE in either LRS or HRS is subjected to a similar read voltage. However, the overall cell NL½ during the write operation degrades, since the selector is turned-on at too low voltage, therefore the dominant cell resistance will be given by the 1R-only at half-bias.

For selector B, increase of V_{th} improves the non-linearity for the full cell at write operation, whereas the R_S needs to be increased as well to avoid read disturb. At a consequence, the full cell RW decreases and more voltage is required for the read and write operations. The read voltage is mainly affected by the V_{th} while the full cell write voltage only depends on the on-state R_S.

As shown in Fig.3.10, the trade-offs between the large full cell RW, low voltage operation and high non-linearity for write operations occur for type-II selector as well, similar to that of type-I selector. Beyond that, read disturbance activates additional constraints for designing type-II selector, which is not an issue when combining the RSE with a type-I selector.

3.2.4 1S1R array level analysis

In the previous section, we analyzed the behavior of single 1S1R cell at device level. In this part, we further consider a full cell array simulation to determine the selector characteristics that are required to achieve the constraints defined in TABLE.3.1, assuming 1Mbit array size. Variability-free approach is employed, which means the selector and RSE behavior, either in LRS or HRS are identical from cell to cell. Read and reset operations are analyzed in the following sections. During the set operation, the 1S1R cell has similar nonlinearity to that of the reset due to the symmetrical 1S, 1R behaviors. Consequently, set introduces constraints similar to that of reset. For this reason, set operation is not discussed in further detail in the following.

3.2.4.1 Type-I selector

The array simulation is carried out using the procedure as depicted in Fig.3.1. We start with the analysis assuming ½-bias scheme.

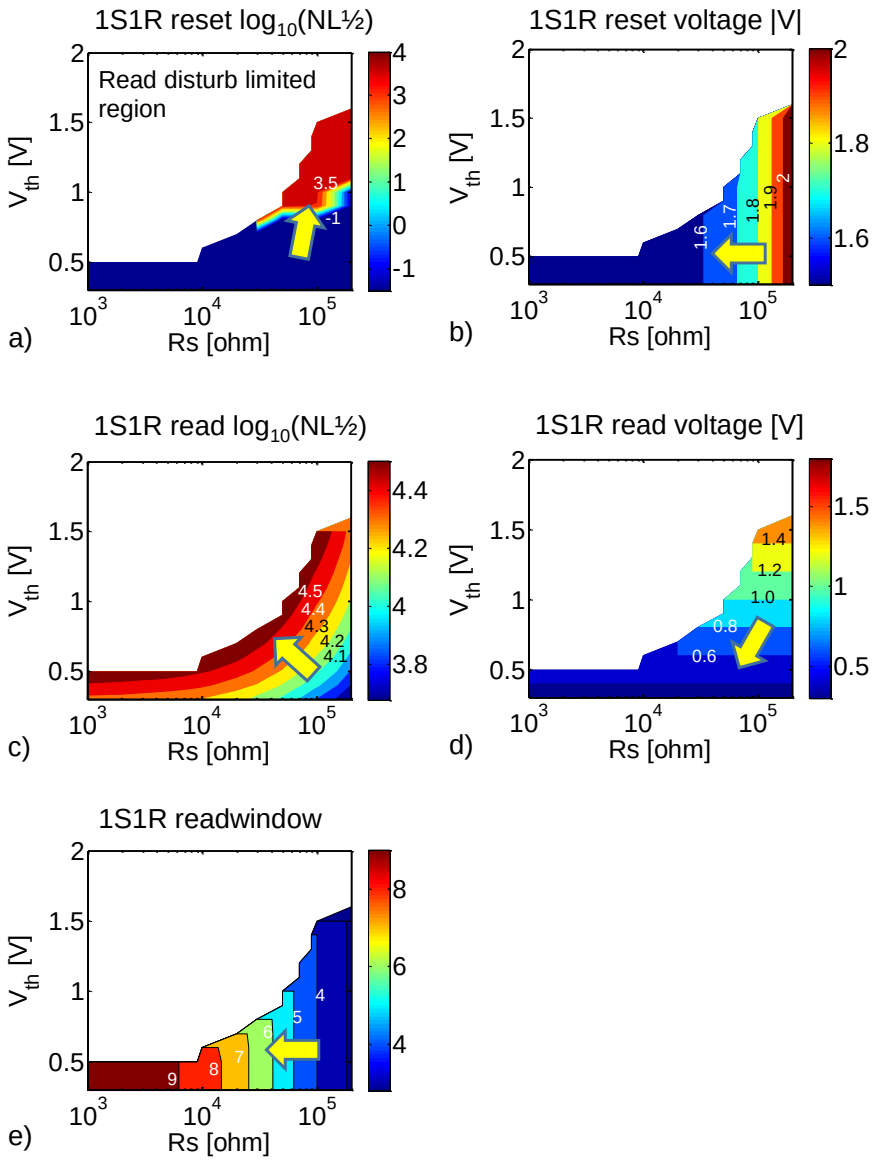


Figure 3.10: *Contour plots for the full cell characteristics (scales on the color bar) (a) reset NL½ (b) reset voltage (c) read NL½ (d) read voltage (e) RW as function of selector parameters: selector R_S (x-axis) and Selector V_{th} (y-axis). NL½ is fixed at 10^4. The arrow shows the best improvement direction for reaching the full cell performance targets. The different arrow directions evidence the tradeoffs for the 1S1R cell configuration.*

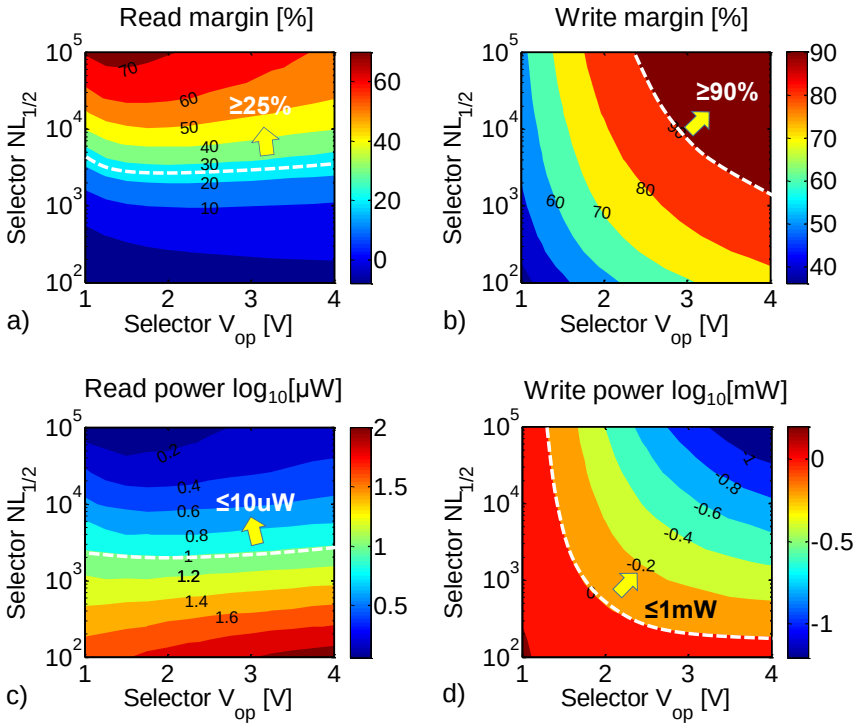


Figure 3.11: *Contour plots for the array performance (scales on the color bar) (a) read margin (b) write margin (c) read power (d) write power as function of selector parameters. ½-bias scheme is assumed. Dash curve shows the min. selector parameter requirements under the array performance constraints.*

The figures-of-merit of array read performance is plotted as function of selector parameters. Selector NL½ from 10^2 to 10^5 and operating voltage range (V_{op}) in between 1V and 4V are within the considered design range. Fig.3.11.(a) shows that the RM is strongly affected by the selector NL½ but much less by V_{op}. The weak V_{op} dependency is due to the fact that, on one hand, increasing V_{op} decreases the RW of 1S1R at cell level (Fig.3.7.e), on the other hand, this improves the 1S1R nonlinearity at read condition (Fig.3.7.c). The RM, however, depends on both RW of the selected cell and the leakage currents from the unselected cells, which are strongly reduced for a cell with high NL½. As a result, the two effects counterbalance each other. The selector NL½ must exceed $2*10^3$ for achieving the RM$\geq$ 25%. Fig.3.11.(b) shows that the WM strongly depends on the selector V_{op}. This is consistent with Fig.3.7.(a), which indicates that large V_{op} and high NL½ selector are required to have large WM.

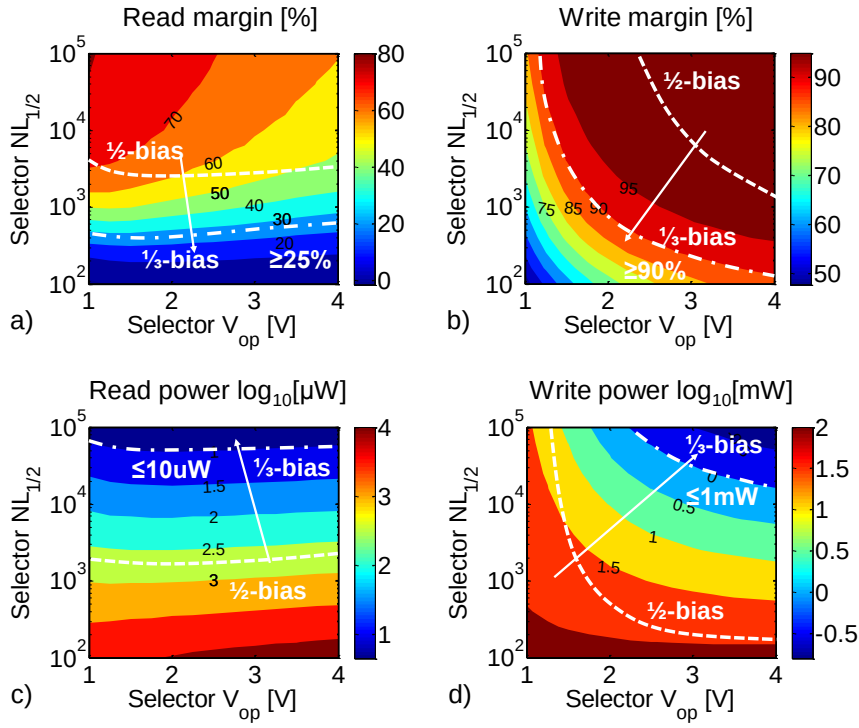


Figure 3.12: *Contour plots for the array performance (scales on the color bar) (a) read margin (b) write margin (c) read power (d) write power as function of selector parameters. Dash curves indicate min. selector requirements based on the ½ and ⅓-bias scheme, respectively.*

Fig.3.11.(c) and (d) plot the relationship between the power consumption and selector characteristics. Although selector with large V_{op} increases full cell operating voltage, it is not necessarily increasing the power consumption because it provides large full cell NL½ and hence reduces leakage of the half- and non-selected cells. Furthermore, we find that there is no trade-off between improving RM/WM and reducing P_W/P_R (e.g. arrow indicates the nearly same improvement direction).

Impact of bias scheme A ½-bias scheme, although commonly used for estimating array size in cross-point array is unlikely to be optimal [115], and other bias schemes should be considered as well. Fig.3.12 shows the results assuming a standard ⅓-bias condition. Compared to the ½-bias scheme, to obtain the same RM and WM, the selector design region meeting both constraints extends (Fig.3.12.a-b). This is due

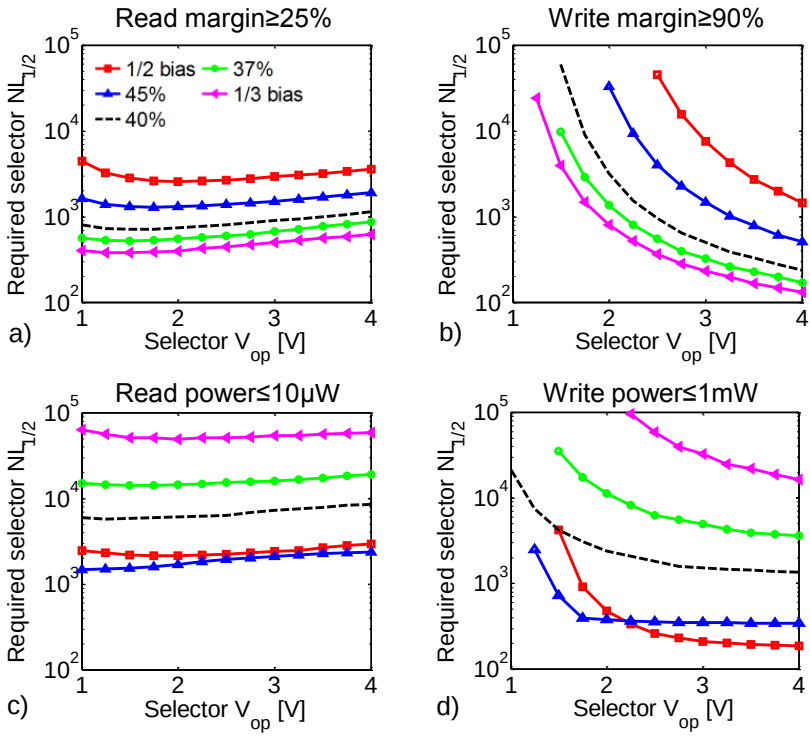


Figure 3.13: *The extracted min. selector requirements under the constraint (a) read margin (b) write margin (c) read power (d) write power for different partially bias scheme from ½-bias to ⅓-bias.*

to the fact that a ⅓-bias scheme reduces the leakage currents on the selected WL and BL, which improves both RM and WM. However, this trades off with the power consumption, since the voltage on the non-selected cell increases. In order to meet the power constraints, selectors with much higher NL½ and operating voltage are required (Fig.3.12.c-d). We sweep bias schemes in between ½ and ⅓-bias and extract the minimal selector parameter requirements for each condition (Fig.3.13). As can be seen (Fig.3.13.a-b), reducing of the partial bias scheme from ½-bias to ⅓-bias allows for RM and WM at lower selector nonlinearity, but this severely increases the power consumption (Fig.3.13.c-d). For selectors with a given V_{op}, the NL½ requirement under different bias schemes can be extracted from Fig.3.13. Under the read performance constraints, an optimized bias on the unselected WL_s and BL_s, i.e. V_{WLNS}~46%V_{dd}, V_{BLNS}~54%V_{dd} (Fig.3.14.a) for the read operation is determined, which yields the lowest NL½ requirement (~2000) for fulfilling both the read operation requirements

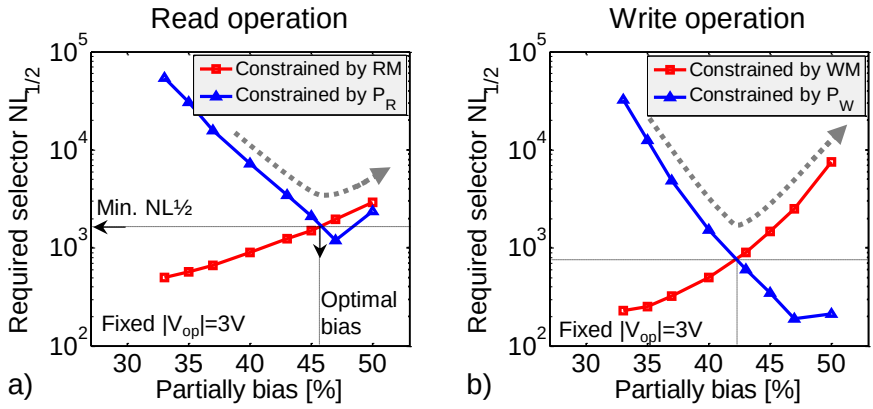


Figure 3.14: *The selector NL½ (at fixed V_{op}=3V) requirement vs. array bias considering (a) read margin and read power constraints (b) write margin and write power constraints. The min. NL½ is achieved at the cross-point for fulfilling both read (or write) operation requirements.*

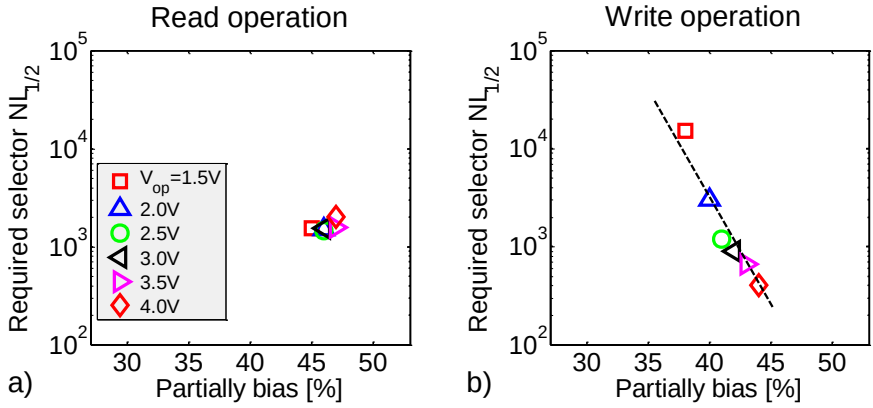


Figure 3.15: *Extracted min. selector NL½ requirements for different V_{op}, considering optimal bias for both (a) read (b) write operation.*

(i.e. RM and P_R). Similar to the read operation, an optimal bias V_{WLNS}~42%V_{dd}, V_{BLNS}~58%V_{dd} can be found for the write operation, resulting in a minimal required NL½ of about 800 (Fig.3.14.b).

The selector nonlinearity requirements depend on the selector operating voltage. The extracted min. NL½ for selectors with different V_{op} are plotted in Fig.3.15. As

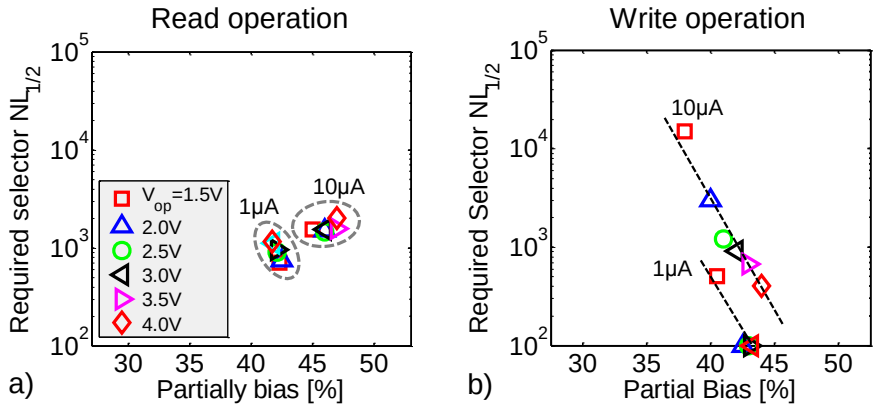


Figure 3.16: *Extracted selector NL½ requirements for 10μA RSE and hypothetical 1μA RSE for both (a) read and (b) write operation.*

can be seen, for the write operation, the min.NL½ requirement reduces from over 10^4 to around 400 if the operating voltage increases from 1.5V to 4V (Fig.3.15.b). This suggests that the operating voltage (V_{op}) is an equivalent important parameter compared to the non-linearity for a selector, especially during the write operation. On the contrary, the NL½ requirements under read operation are much less sensitive to the V_{op} variation (Fig.3.15.a). For a selector with large V_{op}, the read operation is more critical compared to the write operation, which will ultimately determine the minimal nonlinearity requirements for selector. Furthermore, Fig.3.15 also indicates that it is not necessary to use the same bias condition for both read and write operations. For a given selector, an optimal bias which balances performance trade-offs (i.e. WM/P_W and RM/P_R) can be determined for each operation.

Impact of the resistive switching element (RSE)

Low switching current RSE relaxes the drive current requirement for the selector element. Furthermore, the min.NL½ and V_{op} can be reduced as well (Fig.3.16). We model the low current RSE by simply increasing both HRS and LRS resistance of the reference (Fig.3.2), while keeping the other characteristics the same. The I_{drive} of the selector model is adapted as the RSE switching current, e.g. 1μA. The same approach is applied to extract the min.NL½ requirement for different V_{op}, considering optimal bias for both read and write operation. The results show that the min. NL½ requirement relaxes with a low current RSE, especially for the write operation (Fig.3.16.b). With low operating current, the IR voltage drop over the WL/BL interconnects and the power consumption is reduced, which improves the overall write performance. On the contrary, the benefits of lowering the current on the read performance is limited

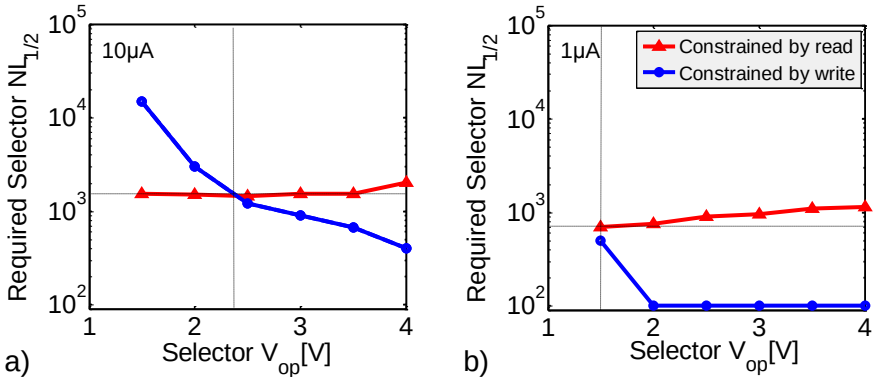


Figure 3.17: *Optimal V_{op} and the min. NL½ for the selector are extracted for combining (a) 10μA and (b) 1μA switching current RSE. The min. requirements for selector is determined by the read operation for the low current RSE. The required NL½ saturates for write operation in (b) is due to limitation of simulation range.*

(Fig.3.16.a). It is because that relative weight of the current is more important for the RM, instead of the absolute current level during the read operation. This result suggests that the read limitation will determine the selector requirements in the low switching current region. As a consequence (Fig.3.17), the min. NL½ decreases from ~2000 to ~800 if the switching current reduces from 10μA to 1μA. Note that, to achieve the min. NL½, the selector V_{op} being larger than 2.4V is required for the 10μA RSE, however, this value becomes smaller (>1.5V) for the 1μA RSE, which indicates potential for lower voltage operation for 1S1R using a low current RSE.

Summary

We investigated the impact of type-I selectors on the overall 1S1R array performance. The results show that the operating voltage V_{op} of the type-I selector is an important parameter. Large V_{op} improves the full cell nonlinearity, especially for write operation. However, this comes at the cost of a reduced 1S1R cell RW and the need for higher voltages during both read and write operations. Simulations show that the required selector NL½ can be strongly reduced by using optimal bias rather than a ½ or ⅓-bias scheme. The use of a RSE with lower switching current would also enlarge the selector design margin. If a low switching current RSE is used, the read operation will become the critical operation to determine the required selector characteristics.

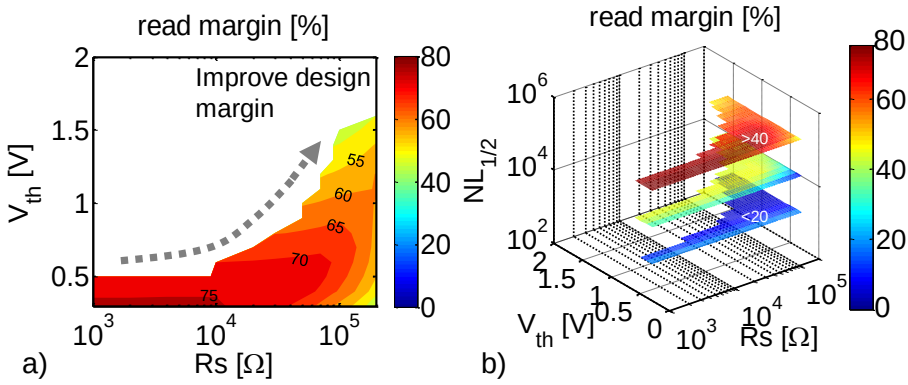


Figure 3.18: *(a) Contour plot for the read margin (RM) as function of R_S and V_{th}, with fixed NL½=10^5. (b) RM as function of R_S, V_{th}, with various NL½=10^3 (bottom), 10^4 (middle) and 10^5 (top).*

3.2.4.2 Type-II selector

In this part, we extend our analysis on the type-II selectors. The same simulation settings and the constraints are applied, as we did before for type-I selectors. The figures-of-merit of the array read performance are plotted as function of selector parameters including the V_{th}, NL½ and R_S.

Assuming a ½-bias scheme, the calculated RM is plotted considering the V_{th} and R_S as free parameters while NL½ is fixed (Fig.3.18.a). The parameters within the blank range causes read disturb (as extrapolated in Fig.3.8), thus must be avoided. We further introduce parameter variation into the selector NL½. Fig.3.18.(b) shows that the NL½ strongly affects the RM, however, it has only limited impact on the design margin for V_{th} and R_S, which means the impact of selector non-linearity on the read disturb is negligible.

To extract the minimal parameter requirements, we re-structure the 3D graph (Fig.3.18.b) and plot the RM as function of NL½ and V_{th} for different R_S (Fig.3.19). The arrow suggests the best RM improvement direction and the dash line shows the min. parameter requirement to fulfill the applied constraint (i.e. RM$\geq 25\%$).

A large R_S is desired as it improves V_{th} design range. However, increasing R_S reduces full cell RW at device level (as we discussed in Fig.3.9.b), which may lead to the RM degradation. To investigate this trade-off, the min. selector parameter requirements (e.g. dash line in Fig.3.19) are extracted considering various R_S (Fig.3.20.a). On one hand, increasing R_S from 1kΩ to 0.2MΩ improves the up-limit of V_{th} from 0.4V to about

1.8V. On the other hand, the minimal required NL½ rises, i.e. for a given V_{th}=0.4V, the required NL½ increases from 4900 to $1.5*10^4$. On the contrary, R_S has limited impact on the selector NL½ requirements extracted from read power constraint (Fig.3.20.b).

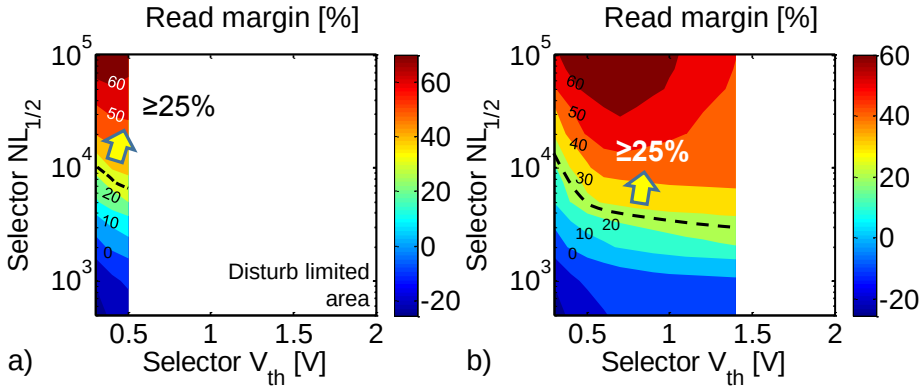


Figure 3.19: *Contour plot for RM as function of selector NL½ and V_{th}, with fixed (a) R_S=1kΩ. (b) R_S=0.1MΩ. Dash curve indicates the min. selector parameter requirement under RM constraint.*

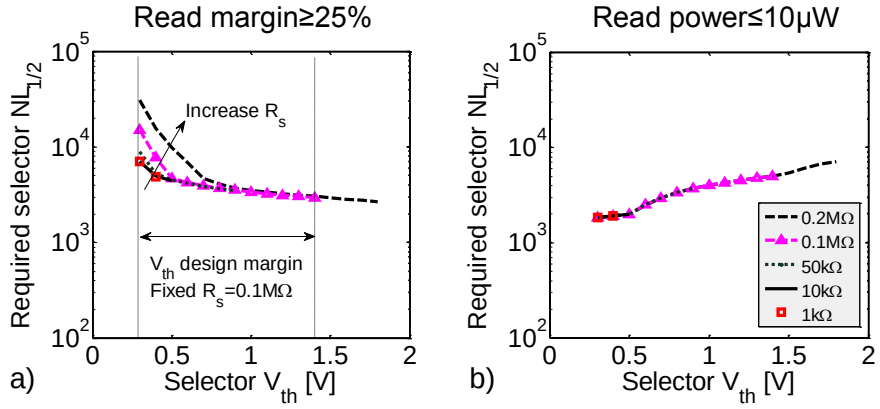


Figure 3.20: *Extracted min. selector parameter requirement under (a) read margin and (b) read power constraint.*

This is because that the read power is strongly affected by the leakage currents from the unselected cells. The leakage currents, however, only depend on the off-state

characteristics of the type-II selectors. Considering R_S trade-off in practice, an 'optimal' R_S of 0.1MΩ is assumed. This R_S leads to a moderate V_{th} design margin (i.e. 0.2V to 1.4V) and low operating voltage (1.8V, as we extracted from Fig.3.9.b). Furthermore, compared to a large R_S value (e.g. 0.2MΩ), the additional NL½ requirement for achieving the same RM is limited (Fig.3.20.a). In the following analysis, we consider the R_S as a fixed parameter (0.1MΩ).

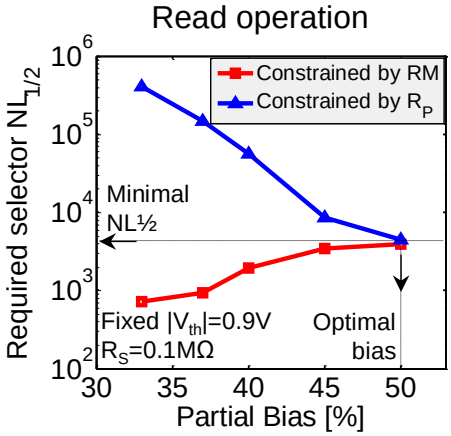


Figure 3.21: *The min.NL½ requirement vs. array bias considering both RM(≥25%) and R_P (≤10μW) constraints. V_{th} is fixed at 0.9V and R_S is fixed 0.1MΩ.*

The previous analysis on type-I selectors (section 3.2.4.1) shows that the array bias scheme is an important parameter which strongly affects the read performance. An optimal bias can be determined, which leads to the lowest selector requirements for fulfilling both RM and power constraints. The same method (e.g. varying bias condition) is applied to the analysis of type-II selectors. Fig.3.21 shows the extracted minimum selector NL½ requirement (for a given V_{th}=0.9V) under different bias schemes. As expected, a ½-bias scheme relaxes the selector NL½ requirement for fulfilling the P_R constraint while a ⅓-bias is preferable for the RM improvement. In this case, an optimal bias is determined by the cross-point for the two curves (Fig.3.21), i.e. at around ½-bias, which leads to the lowest nonlinearity requirements for a selector. The minimum required NL½ for selectors with different V_{th} are extracted. Fig.3.22 shows that a min. NL½ of about 5000 is required for a type-II selector for fulfilling both RM and P_R constraints. The NL½ requirement is almost independent of V_{th} variations.

Unlike the weak dependency of the read operation on V_{th}, V_{th} strongly impacts the write performance. As can be seen in Fig.3.23, small V_{th} degrades WM and increases

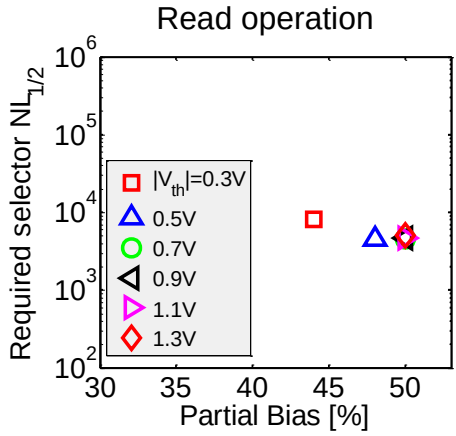


Figure 3.22: *The extracted min.NL½ requirement for selector with various V_{th}. R_S is fixed at 0.1MΩ.*

P_W dramatically. Thus, to improve the overall write performance, large V_{th}'s and high NL½'s are required. During the write operation, since a high program voltage is needed, if the partial voltage bias on the unselected cell is large enough so as to cause a voltage drop over the selector exceeding V_{th}, the selector switches to the on-state and is no longer able to provide selectivity. As a result, the leakage current from the unselected cell mostly determined by the RSE itself, which is linear for both states. Similar results have been observed for type-I selector, when the device has small operating voltage (as discussed in Fig.3.11.b,d). Therefore, choosing a proper voltage, compatible with the RSE is important for both selector candidates, especially during the write operation.

When a ½-bias scheme is assumed, WM is the decisive constraint that determines the minimum selector requirements (Fig.3.23.a), while the power constraint P_W is more critical under an ⅓-bias scheme (Fig.3.23.d). We further extract the minimum selector parameter requirements under different bias conditions (Fig.3.24), using an approach similar to the one for type-I selector.

The result indicates that there is an optimal bias (Fig.3.24), i.e. V_{BLNS}~47%V_{dd}, V_{WLNS}~53%V_{dd}, which gives the minimal required NL½ to fulfill both WM and P_W constraints. The required selector NL½ is strongly affected by V_{th}. To this end, a high V_{th} is preferred, as it relaxes the requirement for NL½. Note that only one point is extracted for the case when V_{th}=0.7V, it is because the required selector NL½ is beyond our simulation range (e.g. NL½=10^5) for the non-optimal bias conditions. Finally, the minimum selector parameters requirements are determined by considering the constraints from both read and write operations (Fig.3.25). An optimal V_{th} of about

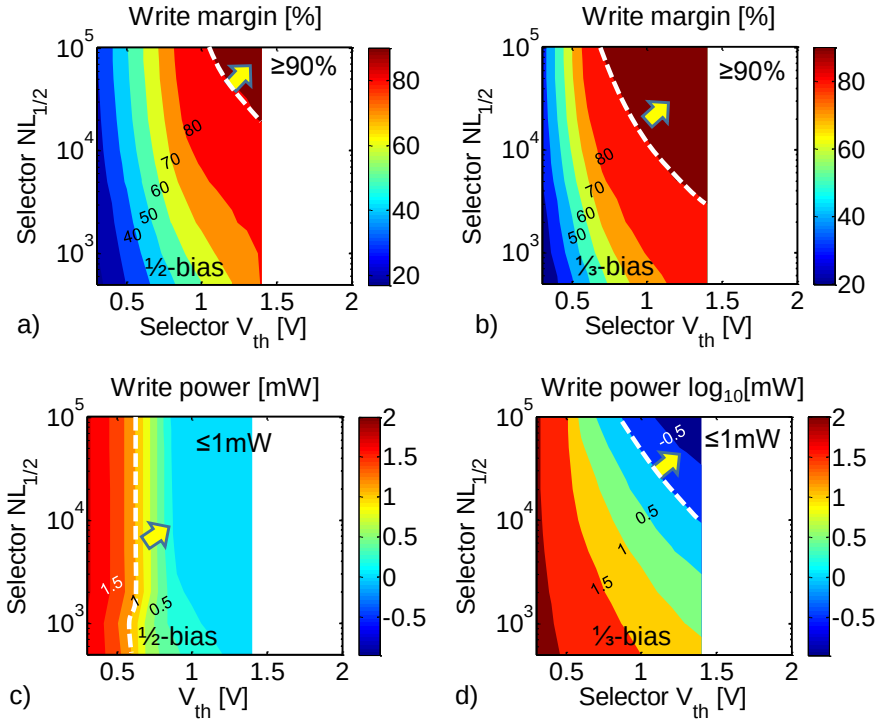


Figure 3.23: *Contour plots for the array performance (scales on the color bar) (a) WM and (c) P_W under ½-bias scheme. (b) WM and (d) P_W under ⅓-bias scheme. R_S is fixed at 0.1MΩ. Blank area indicates the disturb limited region. The dash line indicates the min. required selector characteristics. The arrow suggests the best improvement direction.*

0.9V is found at the intersection of the two curves. Increasing V_{th} beyond this value will not further reduce the NL½ requirement since it is mostly determined by the read operation. Fig.3.25 also suggests the V_{th} design margin, where the lower-limit (i.e. 0.7V) is mostly determined by the write operation constraints. With too small a V_{th}, the selector turns on at too small voltages, therefore it is not able to limit the leakage currents from the unselected 1S1R element. The upper-limit (i.e. 1.4V), however, is mainly limited by the RSE read disturb constraint.

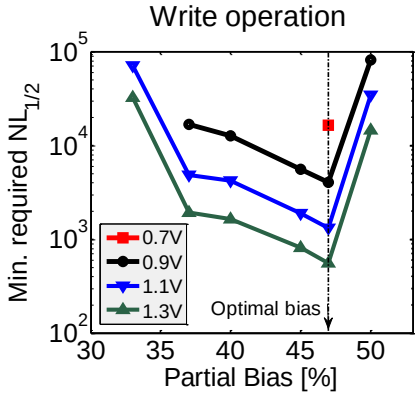


Figure 3.24: *Selector NL½ requirements considering both WM and P_W constraints under various bias conditions. The Min. NL½ is achieved at optimal bias. Small V_{th} below 0.7V leads to large NL½ requirement which is beyond our simulation range.*

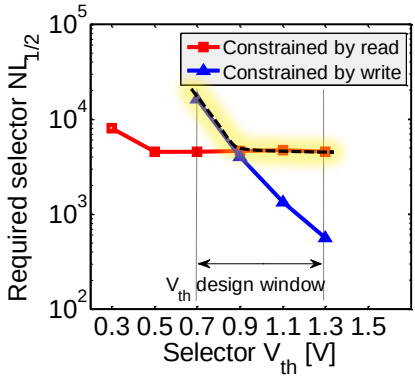


Figure 3.25: *The min. requirements for selector considering both read and write constraints. The red curve (square) is extracted from Fig.3.22 and the blue curve (triangular) is determined from Fig.3.24.*

3.2.5 Summary and benchmark

TABLE.3.7 summarizes the parameters for the default RSE, the extrapolated minimal selector requirements and the extracted operation voltage for the full 1S1R cells. The drive current, non-linearity and voltage compatibility with the RSE are important

aspects when designing a selector.

Table 3.7: The extracted selector parameter requirements targeting for 1Mbit memory array at 10nm cell size

Array size: 1024x1024		**Type-I**		**Type-II**
Default	$I_{switching}$(μA)	1	10	10
RSE	$V_{set/reset}$(V)	±1.5	±1.5	±1.5
	$\|V_{disturb}\|$(V)	0.5	0.5	0.5
	$\|V_{read}\|$(V)	0.1	0.1	0.5
Target	J_{drive}(A/cm^2)	>10^6	>10^7	>10^7
for	V_{op}(V)	>1.5	>2.4	N.A
selector	NL½	>800	>2000	>5000
	$\|V_{th}\|$(V)	N.A	N.A	(0.7,1.3)
	R_S(MΩ)	N.A	N.A	0.1[a]
	I(½V_{op} or ½V_{th})(nA)	1.25	5	2
1S1R	$\|V_{set/reset}\|$(V)	>3	>3.9	1.8

[a] Fixed parameter.

a) The drive current

As a prerequisite, selector must provide enough current to enable switching of the RSE. Interests for type-II selectors mainly come from high on-state current, e.g. most of the reported threshold switching selectors [62, 105, 108, 140, 141] show drive current density of over 10^7A/cm^2. This enables a RSE in the cell with 10μA switching current at 10x10nm^2 cell size. On the contrary, only a few type-I selectors [94, 112] reach that limit. A low current RSE is desired. We find that a low switching current RSE not only relaxes the drive current requirement for the selector element, but the minimal NL½ and V_{op} can be reduced, as well.

b) Nonlinearity

Read operation seems to be more critical than write operation which will ultimately determine the minimal NL½ requirements. Assuming a 10μA RSE, NL½ exceeding 10^3 is essential for both selector categories, which means that the half-bias leakage current should be reduced to below single-digital nA values.

c) Voltage compatibility

The operating voltage V_{op} of the type-I selectors is important. Large V_{op} improves the full cell nonlinearity, especially for the write operation. Consequently, V_{op} being larger than 2.4V is required for the RSE with a program voltage at ±1.5V (10μA). Similarly, V_{th} is important parameter for type-II selectors. Large V_{th} prevents the

selector switching to the on-state for the unselected cells during the write operation. However, an excessive large V_{th} leads to unintentional read disturb. To protect the RSE from disturbance, a large enough on-state resistance R_S is required.

Moreover, we find that the 1S1R full cell operating voltage cannot be very low when combining the RSE with type-I selector, due to the requirement of a large selector V_{op} (i.e. >2.4V). On the contrary, low voltage operation is easier to achieve for type-II selectors, where the full cell program voltage only depends on R_S. In our case, e.g. a voltage of 1.8V is estimated for an R_S of 0.1MΩ.

c) Benchmarking for different selector concepts reported in literature

We consider type-I selectors, namely MSM [139], Varistor [94], M/SiNx/M [89], silicon NPN [81] MIEC [112] and type-II selectors, i.e. OTS [105], FAST [108] and TVS [141]. The I-V characteristics are digitized in Fig.3.26. For all the selectors, we estimate the current assuming the selector is able to deliver 10μA drive current. The extract selector parameters are listed in TABLE.3.8 and TABLE.3.9.

Table 3.8: Extracted Type-I selector parameters

	V_{op}(V)	$NL_{1/2}$	Slope(mV/dec)	J_{drive}(A/cm$_2$)
MIEC	1.2	8*10^4	85	10^7
Varistor	1.6	10^4	282	10^7
MSiM	2.4	260	330	10^6
MSiN$_x$M	2.0	150	330	10^5
NPN	1.6	100	219	10^6

Table 3.9: Extracted Type-II selector parameters

	V_{th}(V)	$NL_{1/2}$	R_S(kΩ)	J_{drive}(A/cm$_2$)
FAST	0.8	10^7	8	5*10^6
TVS	1.3	2360	11	10^7
OTS	2.4	110	9	10^7

MIEC and Varistor selectors have the best performance in terms of high non-linearity and large drive current, however, they are not compatible with the RSE (e.g. program voltage at or larger than $|\pm 1.5V|$) due to their low operating voltage range, which degrades write performance in a 1S1R cell configuration. Among type-II selectors, FAST shows best nonlinear characteristics and proper threshold voltage (e.g. within in the proposed design range). The concern remains the too low on-state resistance, which may lead to read disturbance. For the OTS and TVS selectors, R_S needs to be

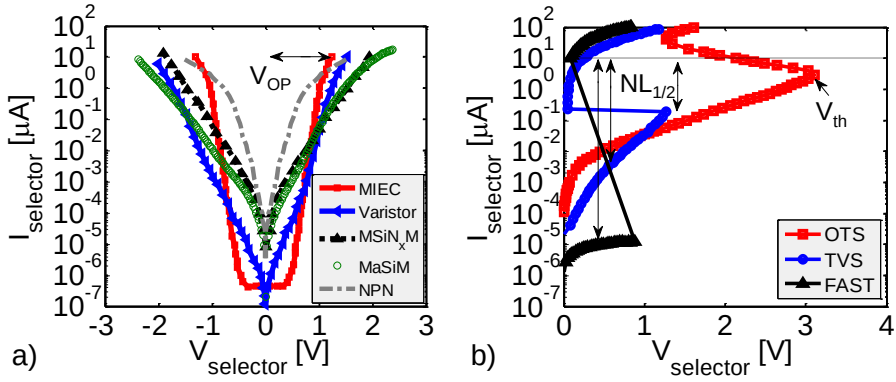


Figure 3.26: *Experimental IV characteristics of (a) type-I selectors and (b) type-II selectors.*

Table 3.10: Selector improvement direction

	Type-I selector
MIEC	Operating voltage
Varistor	Operating voltage
MSiM	Non-linearity, drive current
MSiN$_x$M	Non-linearity, drive current
NPN	Non-linearity, drive current, operating voltage
	Type-II selector
FAST	R_S
TVS	Non-linearity, R_S
OTS	Non-linearity, threshold voltage, R_S

increased as well. Moreover, the NL½ characteristics have to be improved, and a lower threshold voltage is desired for the OTS selector.

Finally, TABLE.3.10 summarizes the key parameters that need to be improved for each considered selectors.

3.3 Resistive switching element requirements extraction

In the last section, we analyze the impact of the selector parameters on the overall 1S1R array performance. The simulation results suggest that the voltage compatibility between the selector and the RSE is important, especially during the write operation. By carefully choosing the voltage parameter of 1S depending on the particular properties of the RSE, the selector NL½ requirements relaxes. In this case, the read operation becomes more critical than write. For this reason, we focus on the read operation in the following study.

Although both RSE and selector affect the readout current in the cross-point arrays, most of literature mainly focused on the impact of the latter, showing that high nonlinearity selector is required for improving the read margin [115, 121, 133]. The requirements for the RSE are only scarcely addressed [133] and it is generally concluded that a large R_{HRS}/R_{LRS} ratio is desired, as this facilitates an easy distinction between the two resistance states, hence improving the read margin. Moreover, with a selector, the resistance ratio of the 1S1R cell will reduce compared to the 1R-only case, suggesting that R_{HRS}/R_{LRS} ratio needs to be increased in order to obtain sufficient full cell read window.

In this section, we present a SPICE analysis on the impact of the RSE parameters on the overall 1S1R array read performance, considering both R_{LRS} and R_{HRS} as free parameters. For a given selector performance, we find that there is an optimal R_{HRS}/R_{LRS} ratio, which improves the overall performance of the read operation in the array. Increasing of the R_{HRS}/R_{LRS} ratio beyond that optimum does no longer improve the read margin. On the contrary, it even degrades it, rendering the effort to excessively open up the R_{HRS}/R_{LRS} ratio of the RS element to be counterproductive. Furthermore, we found that it is more effective to improve the read margin by increasing the selector nonlinearity instead of increasing the on/off resistance ratio.

3.3.1 Simulation settings

The same 2D cross-point analysis framework is employed, assuming the worst case scenario for an 1Mbit array. For simplicity, a fixed ½-bias scheme is applied, as an optimal bias condition, yielding a good trade-off between the read margin and read power consumption. A type-I selector is considered in the 1S1R cell. Symmetrical selector characteristics are assumed, modeled with the same parametrized template (as depicted in Fig.3.3) with fixed parameters. The selector drive current is set at 10μA, operating voltage range V_{op} and half-bias NL½ are fixed at 3V and 1500, respectively, so as to reflect the experimental behavior reported in [127].

The RSE is modeled by assuming Ohmic-behavior for both states, with resistance levels R_{HRS} and R_{LRS}, of which values can be varied independently (free parameters). Using a non-linear RSE causes only marginal difference compared to that of Ohmic-behavior RSE, as we will discuss later. Other RSE parameters, e.g. the set/reset voltages are not considered as they are irrelevant to the read operation. The I-V characteristics of the full 1S1R cell are constructed by combining a fixed selector template and a variable RSE model. The read voltage value on the full cell is determined by imposing the condition that the voltage drop on the RSE equals to -0.1V, when the RSE in the LRS.

3.3.2 Impact of the on/off resistance ratio

We sweep free the RSE parameters and plot the array read performance as function of R_{HRS} and R_{LRS}. The two parameters strongly impact the read performance. Fig.3.27 shows the trade-offs for achieving both large RM and low read power consumption (P_R). Low R_{LRS} is required to improve the read margin (RM), however, this leads to high LRS readout current thus increasing P_R. An optimal R_{LRS} can be determined, resulting in the lowest P_R, which maintaining acceptable RM. Fig.3.27.(a) also indicates that the RM improvement by increasing R_{HRS} will saturate and eventually decrease, revealing that for a given R_{LRS}, choosing an optimal R_{HRS} is required for maximizing the RM. This conclusion holds, for increasing selector non-linearity (discuss later in Fig.3.30).

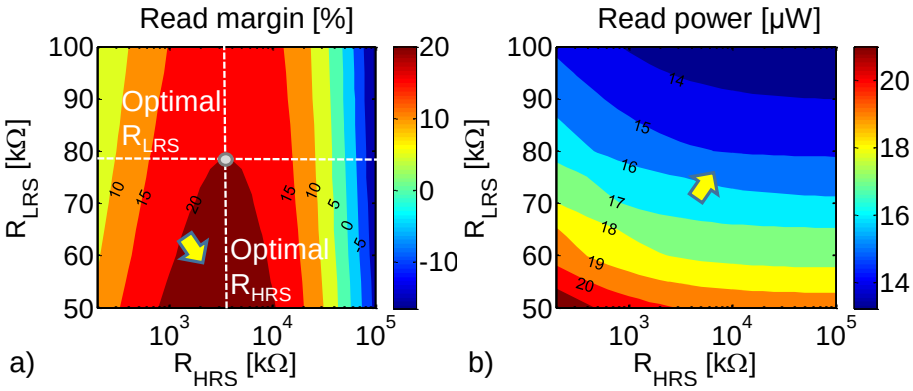


Figure 3.27: *Contour plots for array performance (scales on the color bar) (a) RM (b) P_R as function of R_{HRS} and R_{LRS}. The arrows show the best performance target. Different direction suggests the tradeoffs for read operation. To balance RM and P_R, optimal R_{LRS}~80kΩ, R_{HRS}~3MΩ and optimal resistance ratio of about 40 is determined at the cross-point of dash line.*

To understand this RM degradation effect caused by large R_{HRS}, RSE with different R_{HRS} are compared by analyzing their full 1S1R behavior, Fig.3.28.

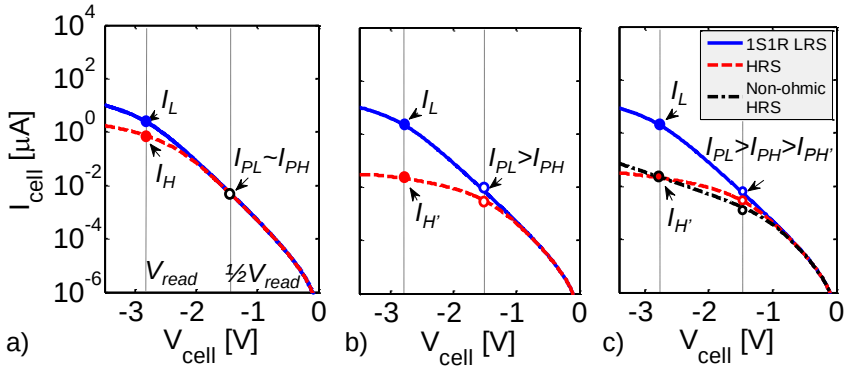


Figure 3.28: *Constructed 1S(fixed)1R behavior. 1R: R_{LRS} (50kΩ) (a) R_{HRS}=500kΩ (b) R_{HRS}=5MΩ. (c) Non-linear R_{HRS}. G_{HRS}=1/R_{HRS}, α=0.1, β=3. β determines the non-linearity. I_L: 1S1R$_{(LRS)}$ readout current; I_H: 1S1R$_{(HRS)}$ readout current; I_{PL}: 1S1R$_{(LRS)}$ half-bias leakage current; I_{PL}: 1S1R$_{(HRS)}$ half-bias leakage current.*

A first order RM estimation, which neglects the impact of wire resistance for the worst case data pattern is given by

$$RM \cong \frac{(I_L + n \cdot I_{PH}) - (I_H + n \cdot I_{PL})}{I_L + n \cdot I_{PH}} \tag{3.5}$$

where I_L and I_H is the 1S1R cell readout current, I_{PL} and I_{PH} refers to the 1S1R cell leakage current at half-bias when 1R in the LRS and HRS, respectively. n is the number of half-selected cells per bit-line (i.e. 1023 in this case). As can be seen in Fig.3.28.(a), if R_{HRS} is smaller compared to $R_{selector}$ at half V_{read} bias, the leakage currents given by the bit-line half-selected (BLHS) cells is limited by selector element, i.e. I_{PL}~I_{PH}=I_P. Therefore, equation (3.5) simplifies to,

$$RM \cong \frac{(I_L - I_H)}{I_L + n \cdot I_P} = \frac{\Delta I_{SEL}}{I_L + n \cdot I_P} \tag{3.6}$$

In this case, large R_{HRS} reduces I_H thus improving RM, as the difference between I_L and I_H (i.e. ΔI_{SEL}) becomes larger. Therefore, increasing R_{HRS} initially improves RM (Fig.3.27.a).

However, if R_{HRS} becomes too large, leakage current of the BLHS cells is limited by the RSE (i.e. R_{HRS}) instead of the selector, I_{PL}>I_{PH} (Fig.3.28.b). In other words, the

selector element can no longer sustain the large R_{HRS} increase. Thus, the RM can be rewritten as,

$$RM \cong \frac{\Delta I'_{SEL} - n \cdot (I_{PL} - I_{PH})}{I_L + n \cdot I_{PH}} \tag{3.7}$$

The term n·(I_{PL}-I_{PH}) leads to RM degradation, especially important for high R_{HRS} and large array size.

Considering the fact that RSE commonly has non-ohmic I-V behavior in the HRS, we further express this characteristics by introducing a non-linear item [133],

$$I(V) = \alpha \cdot G_{HRS} \cdot sinh(\beta \cdot V) \tag{3.8}$$

G_{HRS} is the conductance and α, β are the fitting parameters. Assume that R_{HRS}(Ohm) equals to the R_{HRS}(non-Ohm) at the readout voltage, this results in the same $\Delta I'_{SEL}$. The R_{HRS}(non-Ohm) shows higher resistance when reducing the bias while R_{HRS}(Ohm) remains constant. Consequently, the half-bias leakage current (I'$_{PH}$) of non-Ohmic is lower than that of Ohmic (Fig.3.28.c), causing additional RM degradation. P_R, however, is decreased due to a reduction of the half-bias leakage current. Fig.3.28.(c) suggests that although there is a difference between non-Ohmic and ohmic R_{HRS}, the impact is limited. As a consequence, for simplicity, ohmic resistance is used in the following analysis.

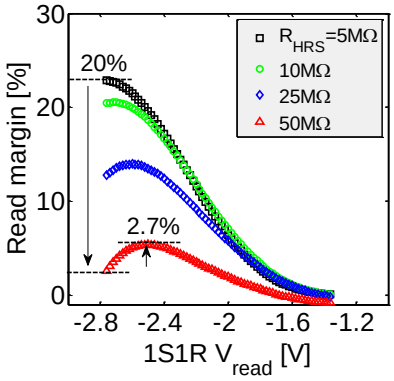


Figure 3.29: *Increasing R_{HRS} from 5MΩ to 50MΩ degrades RM by 20%, a RM gain of only about 2.7% is observed by optimally choosing a smaller read bias at |2.5V|.*

Reducing |V_{read}| to values where the selector resistance is still the dominant component of the cell resistance at half bias limits the RM degradation, Fig.3.29. By optimally choosing a read bias (i.e. ~-2.5V), a RM gain of only 2.7% is obtained compared to

that of read at ~-2.8V (i.e. voltage drop over RSE equals to -0.1V when the RSE in the LRS). Such a limited improvement can hardly compensate for the 20% degradation due to large R_{HRS}. Further reducing the read bias decreases the on/off read window, leading to an even worse read margin. Although reducing the bias on the half-selected cells, e.g. using ⅓-bias scheme improves the RM, this trades off with the read power consumption [50, 134]. In an ½-bias scheme, a large number of NS cells (1023^2) are subjected to higher voltages (~-⅓V_{read}), compared to an ½-bias scheme (~0V), which leads to significant power increase.

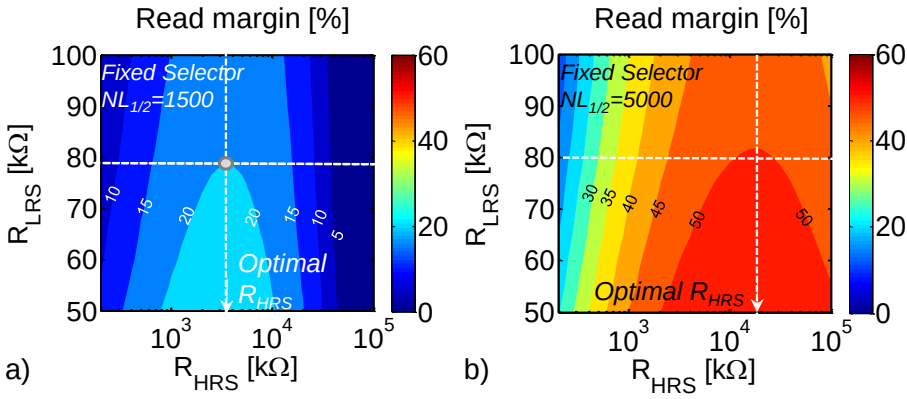


Figure 3.30: *Contour plots for RM (scales on the color bar) as function of R_{HRS} and R_{LRS}. (a) Selector NL½=1500 (b) Selector NL½=5000.*

Such RM degradation due to high R_{HRS} is a common effect (Fig.3.30). For a given selector characteristics, an optimized R_{HRS} and R_{LRS} can be determined to maximize the overall RM, regardless of the NL½ value. However, a highly non-linear selector has large resistance at small bias, thus optimal R_{HRS} can be increased with it, as long as selector dominates the half-bias leakage. The extracted optimal R_{HRS} (left axis) and the optimal on/off state ratio (right axis) are plotted in Fig.3.31.(a), assuming that a (fixed) R_{LRS} equals to 80kΩ. This increased optimal R_{HRS}/R_{LRS} ratio improves the RM. However, the benefit is limited. As seen in Fig.3.31.(b), considering a selector with half-bias nonlinearity of 10^4, improving R_{HRS}/R_{LRS} from 40 (i.e. 3MΩ/80kΩ) to its optimal value 600 only increases the RM by 6.7%. This suggests that selector non-linearity becomes the most important parameter, rather than the RSE optimal on/off resistance ratio.

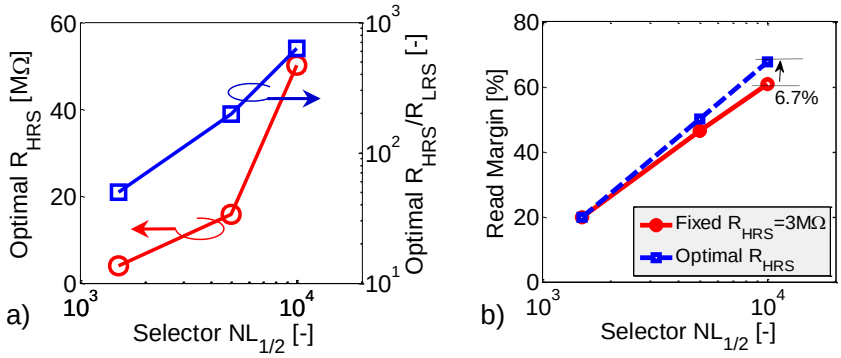


Figure 3.31: *(a) Selector with high non-linearity improves optimal HRS resistance for RSE. R_{LRS} is fixed at 80kΩ. (b) High R_{HRS}/R_{LRS} and large selector non-linearity contribute to RM improvement. The benefits of increasing R_{HRS}/R_{LRS} for RM is limited.*

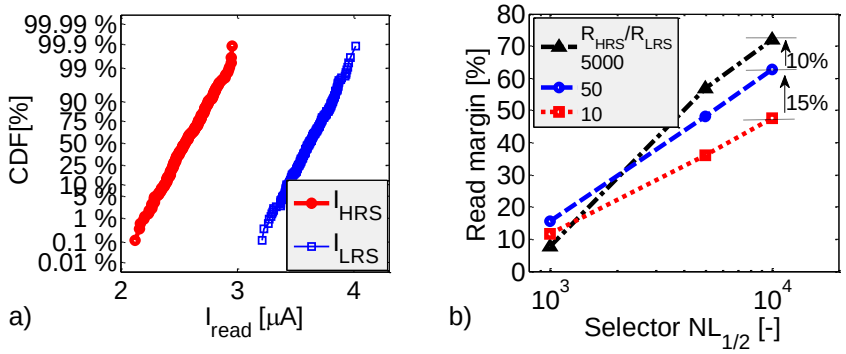


Figure 3.32: *(a) Readout current distribution for Selector NL½=1000, R_{HRS}/R_{LRS}=5000 with random data pattern. Worst case RM is calculated from the tail. (b) Tail-to-tail RM for RS elements with different on/off ratio. R_{LRS} fixed at 80kΩ.*

In the previous analysis, the worst case data pattern is assumed. This leads to a minimal difference in the readout current, which highlights the RM degradation effect. We further investigate the impact of data pattern randomness [122, 134]. Different R_{HRS}/R_{LRS} ratio, 10, 50 and 5000 are analyzed, to mimic typical resistance ratios

for oxide-based RRAM [17], [142] and Cu-based CBRAM [143]. Fig.3.32.(a) shows broad readout current distribution for both states, in contrast to [127], where tight distributions are obtained when the R_{LRS} and R_{HRS} are randomly distributed in the array. This large spread out of the readout current is due to a too large R_{HRS} compared to the selector resistance at low bias, i.e. the selector is not able to select for that R_{HRS} at a specific bias. As a result, RM degradation occurs. On the other hand, with a highly non-linear selector, the RM improvement by increasing the resistance ratio is initially large then becomes limited. For instance, a 15% improvement is observed when the on/off ratio increases by a factor of 5 only, while a further increase of the on/off resistance ratio by a factor of 100, will only improve the RM by about 10%, for a selector half-bias non-linearity of 10^4.

3.3.3 summary

In this part, we investigated the impact of the RSE resistance on the overall 1S1R read performance. The results show that small R_{LRS} improves the read margin at the cost of raising power consumption, while increasing R_{HRS} initially improves the read margin followed by degradation. Thus, optimally choosing R_{HRS} and R_{LRS} is required to maximize read margin as well as to limit the power consumption. To further improve the read performance, a selector with high non-linearity is required. In this case, selector non-linearity becomes a more important parameter than the RSE optimal resistance ratio. Therefore, pursuing optimization of the RSE towards excessively large R_{HRS}/R_{LRS} ratio, may not be justified from a read performance (read margin) improvement point of view.

3.4 Conclusion

A comprehensive high level circuit simulation is performed to investigate the impact of 1S and 1R parameters on the overall cross-point array performance. By assuming an ideal RSE, the requirements are extracted for type-I and type-II selectors using parameterized characteristics for an array with a reference (fixed) size of 1Mbit, considering constraints corresponding to both read and write operations. We find that the read operation is more critical than write, to determine the minimal selector parameter requirements. For type-I selectors, the operating voltage (V_{op}) is an important parameter. A large V_{op} improves the full cell nonlinearity, especially for the write operation. However, this comes at the cost of a reduced 1S1R read window and the need for higher voltages during the read and write operations. Similar full cell performance trade-offs are found as well, when designing the threshold voltage (V_{th}) and on-state resistance (R_S) for the type-II threshold switching selectors. Compared to

the type-I device, the advantage of using type-II selector is that it is more favorable to low operation voltage. However, challenge remains the limited parameter design margin due to the read disturb issue for the RSE in the cell.

Taking the extrapolated selector requirements as reference, we benchmark the suitability of various selector concepts reported in the literature and identify the main improvement directions for each considered case.

Furthermore, we investigated the impact of the RSE on/off resistance on the 1S1R read performance. Contrary to the conclusion made by previous work that a large R_{HRS}/R_{LRS} ratio is always desirable for improving read margin at array level, we show that for a given selector, an optimal resistance ratio can be determined, which gives the best read performance. This suggests that pursuing optimization of the resistive memory towards excessively large R_{HRS}/R_{LRS} ratio is not necessary. On the contrary, it is more effective to improve the read margin by increasing the selector nonlinearity instead of increasing the on/off resistance ratio.

Chapter 4

Metal/Amorphous-Silicon/Metal (MSM) selector

4.1 Introduction

In this chapter, a novel Metal/Silicon/Metal (MSM) selector using ultra-thin undoped amorphous silicon (a-Si) is proposed for resistive-RAM applications. In contrast to a conventional MSM structure with doped Si, acting as back-to-back Schottky diode, the doping-free a-Si behaves as a low bandgap insulator and provides bidirectional non-linear characteristics by tunnelling conduction. The doping-free a-Si structure alleviates the dopant-induced variability concerns for ultra-scaled devices and eliminates the need for a dopant-activation anneal. The new selector shows a high current drive (>1MA/cm^2), high non-linearity, fast switching speed (<1ns) and excellent reliability.

This chapter is organized as follows. In section 4.2, we introduce the concept of the proposed MSM structure. The capability of MSM is investigated by an initial TCAD device simulation and the doping-free concept is evaluated by comparing the experimental results of doped and undoped devices. In section 4.3, we propose several optimized MSM structures and show how the performance can be improved by both energy barrier modification and process engineering. In section 4.4, we further investigate the device reliability under electrical and thermal stress. From the experimental observations, we expect that trap generation in the a-Si layer during electrical stress could be responsible for the selector degradation, affecting its non-

linearity. To confirm the feasibility of using the new MSM selector for 1S1R cross-point array, circuit simulations have been performed, using the analysis framework introduced in Chapter 2. The simulation results are discussed in section 4.5. The conclusion of this chapter is summarized in section 4.6.

4.2 Metal/Silicon/Metal (MSM) selector

4.2.1 Basic of Schottky barrier

The Metal-Semiconductor (M/S) rectifying system [144–149] has been studied over years. It is widely accepted that a potential barrier (e.g. known as Schottky barrier [145]) is formed at the M/S interface, which is responsible for a non-linear current-voltage (I-V) characteristics. Fig.4.1.(a) shows the band diagram of a high workfunction (W_F) metal and n-type semiconductor in a separate system. When connecting them together (Fig.4.1.b), electrons will flow from the semiconductor to the metal. Eventually, the Fermi-levels of the metal and semiconductor are lined up in equilibrium (e.g. net charge flow equals to zero). The Fermi-level in semiconductor is lower than the one in the metal by an amount of [qϕ_m-q(χ+ϕ_n)], where the W_F of metal qϕ_m is defined as the energy difference between vacuum to its Fermi-level, qχ is the electron affinity of the semiconductor and ϕ_n is the energy difference between the conduction band energy E_c of the semiconductor and its Fermi-level. Finally, a potential barrier is formed at the M/S interface namely the Schottky barrier. In the ideal case, e.g. neglecting interface states, the barrier height is given by,

$$\phi_b = q(\phi_m - \chi) \tag{4.1}$$

whose value is simply represented by the difference between metal W_F and the electron affinity of semiconductor.

Meanwhile, a depletion layer is formed inside the semiconductor region, which is similar to that of an abrupt p+n junction [150] (e.g. metal serves as p+). After joining the metal and n-type semiconductor, electrons diffuse from semiconductor to metal leaving fixed ions with positive charges at the surface. The width of this space charge region is given as:

$$W = \sqrt{\frac{2\varepsilon_s}{qN_d}(\psi_{bi} - V_a - \frac{kT}{q})} \tag{4.2}$$

where ε_s is the permittivity of silicon, N_d refers to doping concentration, ψ_{bi} is the built-in potential in the equilibrium condition given by the workfuction difference between metal and semiconductor, V_a is the external applied voltage on the metal.

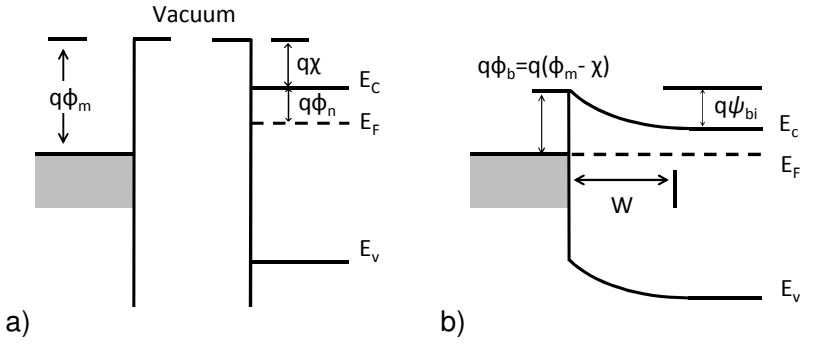


Figure 4.1: *Band diagram of a Metal-Semiconductor contact [148] as separate system (a) and when brought into contact (b).*

4.2.2 MSM selector concept

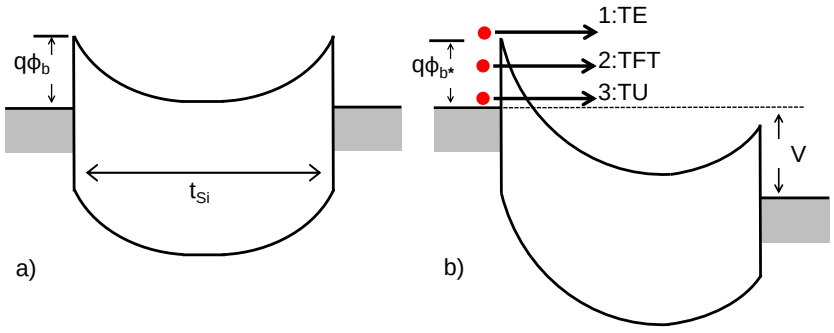


Figure 4.2: *Band diagram of conventional Metal-Silicon-Metal (MSM). (a) at zero bias. (b) being biased. TE: Thermal emission. TFT: Thermal-field tunnelling. TU: tunnelling.*

The conventional Metal/Silicon/Metal (MSM) structure consists of a thick doped silicon layer sandwiched between two metal electrodes. This structure behaves as a back-to-back double Schottky diode (Fig.4.2.a). When an external voltage is applied (Fig.4.2.b), one barrier is under the reverse bias while the other one is under the forward bias. The Current-Voltage (I-V) characteristics are determined by the carriers transported across the reversed biased barrier, i.e. the dominant energy barrier seen by electrons.

According to the thermionic-emission theory [151], for an ideal Schottky barrier, the current density at reversed bias is determined by the barrier height at M/S interface, value of which is constant at any bias. However, in practice, its departures from the ideal behaviour is observed, due to the following three reasons: firstly, the image-force lowers the actual barrier height for electron emission, leading to a decrease of the effective barrier height ($\phi_b{}^*$) with increasing external electric field. This, enhances the thermionic emission current (TE), Fig.4.2.(b). Secondly, a reverse bias can cause the barrier width to become thin enough for tunnelling [152] (TU), Fig.4.2.(b), which exponentially depends on the barrier height and thickness. Thirdly, thermal-field tunnelling (TFT), Fig.4.2.(b), can also occur, i.e. the electrons are thermally excited then tunnel through the barrier which is thinner than the one seen by the pure tunnelling electrons (TU). These current transport processes yield a strong non-linear I-V. Thus, the MSM structure could potentially meet the most stringent requirements for selectors in the cross-point RRAM applications.

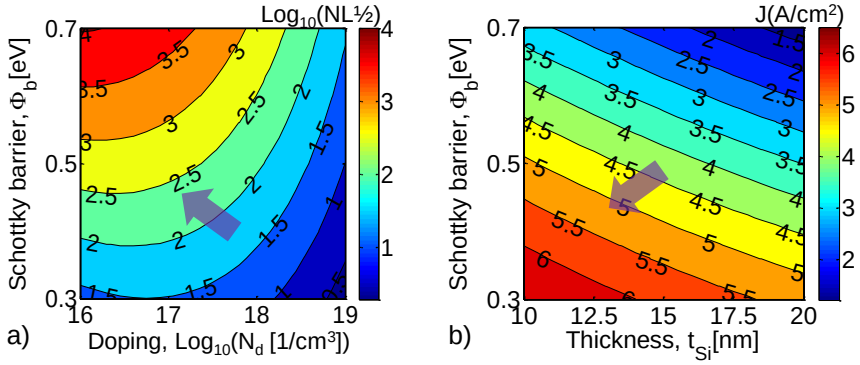


Figure 4.3: *(a) RSM contour plot of the half bias NL½ estimated at 2V, as a function of doping (x-axis, $log_{10}(N_d)$), and M/S barrier height (y-axis, ϕ_b). Contour plot for silicon thickness t_{Si}=15nm. (b) Contour plot of the drive current $log_{10}(J)$ at 2V, as a function of t_{Si} and ϕ_b. Contour plot for a doping of 3*10^{17}/cm^3.*

To investigate the potential of the device, we employ a symmetric MSM structure, on which device simulation is carried out, using a commercial TCAD simulator Sentaurus [153]. The M/S barrier height (ϕ_b), silicon thickness (t_{Si}) and doping concentration (N_d) are considered as variable parameters. The selector performance is assessed by analyzing the I-V characteristics, from which the current density at a fixed voltage (e.g. 2V) and the corresponding half bias non-linearity NL½=J(V_a=2V)/J(V_a=1V) are extracted to build second order response surface models (RSM) [154]. In this study, we consider only the thermionic emission (TE) and electron tunnelling (TU) as the current transport mechanisms, where the thermal-field tunnelling (TFT) is excluded.

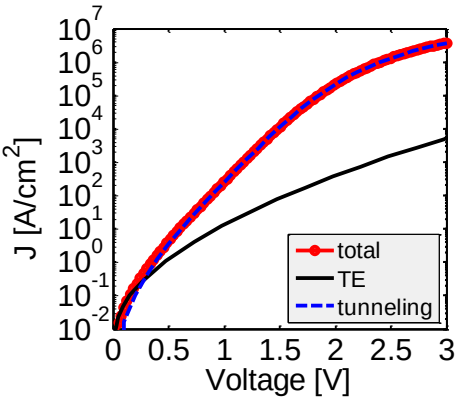


Figure 4.4: *TCAD simulated device I-V characteristics. Tunnelling current is the dominant for the total current. Main simulation parameters:* ϕ_b*=0.5eV,* t_{Si}*=15nm,* N_d*=*10^{16}*/cm*^{3}*,* m^**=0.5*m_0.

From practical fabrication point of view, the total selector stack thickness should be minimized. A low aspect ratio improves manufacturability, e.g. reduces the etching time and profile. Due to this concern, the silicon thickness is kept in the range between 10nm to 20nm in this simulation.

The RSM contour plot result shows that the half-bias NL½ increases with barrier height and with decreasing doping concentration, Fig.4.3.(a). On the other hand, the drive current increases with decrease of barrier height and silicon thickness, indicating a drive current, non-linearity trade-off, Fig.4.3.(b). Although such trends are somewhat to be expected, it is important to notice that for (ϕ_b) of about 0.5eV and thin silicon films, the dominant transport mechanism is electron tunnelling (Fig.4.4). The impact of the doping vanishes when it decreases to below 10^{17}/cm^3. The limited impact of the low doping on the non-linearity can be understood in relation to the Debye length, which, for our thin silicon films, yields a potential barrier profile essentially resembling that of an insulating material (Fig.4.5.a), e.g. the silicon layer is fully depleted. In this case, a low-doped and doping-free device with large barrier width leads to a reduction of the tunnelling current, which improves overall device non-linearity. At large bias, the drive current is almost unaffected thanks to a thin Si film thickness (Fig.4.5.b).

Through the initial TCAD simulation, the feasibility of MSM device is evaluated. We find that highly doped silicon is not suitable for improving the non-linearity, as it reduces the tunnelling barrier width, causing an increase of leakage current, which is not desired for selector application. While a lightly doped thin silicon film is fully depleted, resulting in a limited impact of doping on the device non-linearity. Thus,

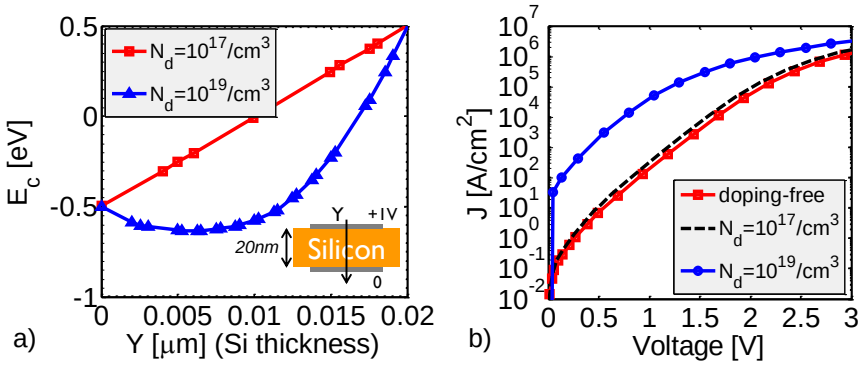


Figure 4.5: *(a) Simulated conduction energy band for MSM devices with different doping concentration. The silicon layer is fully depleted for low doped silicon. (b) Simulated I-V characteristics for high, low doped and doping-free devices. Main simulation parameters:* ϕ_b*=0.5eV,* t_{Si}*=20nm,* m^**=0.5*m_0.

a doping-free MSM can be employed, for achieving a similar performance. From a practical perspective, a doping-free approach would alleviate the issue of increasing dopant fluctuations associated with ultra-scaled devices. A dopant density of 10^{18}/cm^3 translates to only 1 dopant on the average in a structure with feature size 10nm and an aspect ratio of 1. This renders a doping-controlled M/S interface as an unreliable approach for practical implementations.

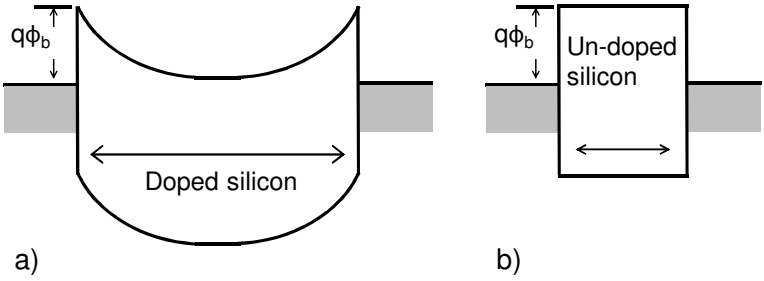


Figure 4.6: *(a) Band diagram of the conventional MSM selector (at no bias), with doped Si, rectifying as a back-to-back Schottky diode. b) Band diagram of the proposed MSM selector, with ultrathin undoped a-Si, which behaves as a low-bandgap tunnel dielectric.*

In summary, we propose a new MSM device using an ultra-thin and doping-free amorphous silicon layer, which behaves as low-bandgap tunnelling dielectric (Fig.4.6.b). Initial TCAD simulation results suggest that the device is able to provide both high drive current and large non-linearity, which could be a promising candidate for RRAM selector applications.

4.2.3 Proof of concept

Crossbar structure TiN/amorphous-Silicon(a-Si)/TiN devices were processed in an integrated process [17], which yields device sizes of various areas ranging from 1x1μm^2 down to 40x40nm^2.

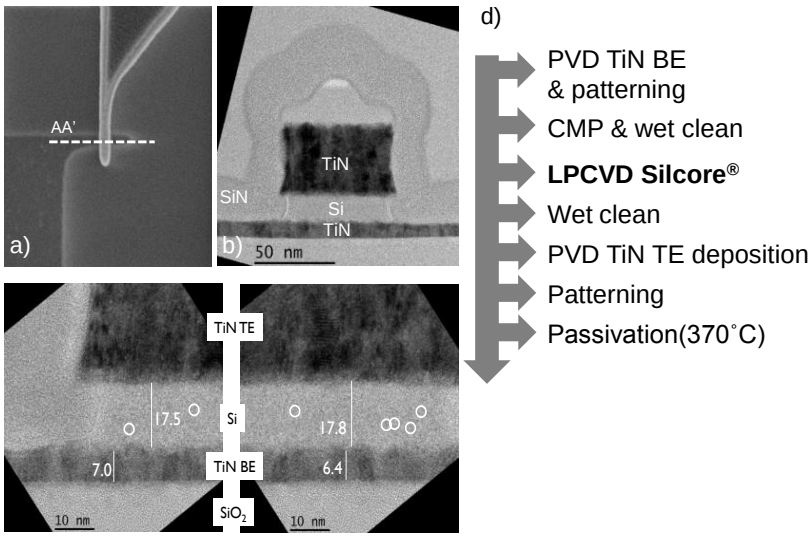


Figure 4.7: *(a) SEM top-view of a 60x60nm^2 crossbar structure. (b-c) TEM cross-section of the crossbar Silcore® based MSM device. (d) Process flow for corssbar MSM selector devices.*

The bottom electrodes (BE) were deposited by room temperature sputtering (PVD). After CMP (Chemical Mechanical Planarization) process and TiN BE patterning, thin 15nm silicon layer was deposited by Silcore® process [155], for undoped and phosphorus-doped silicon film, respectively. Silcore® technique enables an in-situ doping during the silicon film growth, under a low pressure chemical vapor deposition (LPCVD) at 450°C. Right after silicon film deposition, dopant activation anneal (AA)

at 850°C for 1000s was performed for the doped device. Then a wet clean was applied and the top electrode (TE) TiN was deposited by PVD subsequently. The patterned crossbar structures were afterwards passivated in a low-temperature process scheme, not exceeding 370°C. Fig.4.7.(a) shows a top-view scanning electron microscopy (SEM) image of the crossbar structure, and the Transmission electron microscope (TEM) cross-section schematics of the doped Si MSM structure are given in Fig.4.7.(b-c). The TEM picture indicates a large proportion of Si-layer remains amorphous and the presence of a few nanocrystals features are observed in the a-Si matrix (some of them are encircled). Note that a thin interfacial layer might be present between a-Si and TE due to a vacuum break between the Si and TiN deposition, which is not well-controlled, and expose top Si surface to ambient atmosphere. However, this thin layer is not observable due to roughness of top TiN/Si interface and to the lack of contrast for TEM pictures. TABLE.4.1 summarizes the splits information for the MSM devices and general process flow is summarized in Fig.4.7.

Table 4.1: MSM devices split table (impact of doping)

Splits	**BE**	**Dielectric**	**TE**	**Doping(/cm^3)**	**Thermal budget (°C)**
D1	TiN	15nm Silcore®	TiN	undoped	370
D2	TiN	15nm Silcore®	TiN	$8*10^{18}$	850

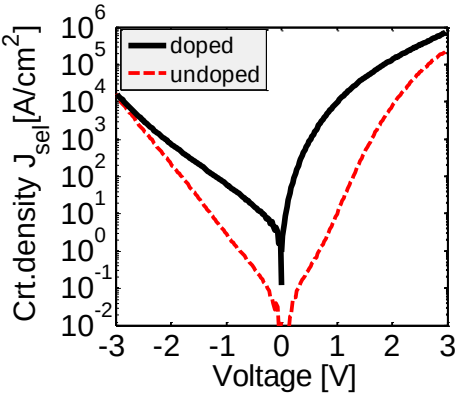


Figure 4.8: *Comparison of doping-free (D1) and doped (D2) 15nm thick Silcore® MSM devices. Cell size: 40x40nm^2.*

Fig.4.8 plots the I-V characteristics for both doped and undoped Silcore® devices. As can be seen, compared to the doped MSM (D2), the doping-free device (D1) shows

much less leakage current at low bias while the difference attenuates at large bias, generating great non-linearity improvement. This trend is in line with the previous TCAD simulation prediction (Fig.4.5.b), indicating that doping-free is a preferable approach for thin film silicon selector achieving high performance. Meanwhile, strong asymmetrical I-V characteristics are observed for the doped device, while the symmetry is much improved for a doping-free device. This implies that the asymmetry I-V may comes from a non-uniform dopant distribution through the silicon layer, resulting in different barrier shape seen by electrons injecting from different polarities. The remaining asymmetry presented in the doping-free device is possibly due to the following reasons:

(a). Considering the vacuum break between Si/top TiN deposition is not well-controlled, a thin SiO_2 interfacial layer might be presented at the interface. This could increase the barrier the electrons have to tunnel through, so that the current at a given bias is reduced, when injecting from top interface.

(b). Due to the oxide CMP stopping on the bottom electrode, before Silcore® deposition, the surface of bottom TiN may be oxidized and form a thin TiON layer, which leads to difference between the bottom and top M/S interface.

(c). The geometry asymmetry is caused by the crossbar test vehicle. The local electric field enhancement effect may result in I-V discrepancy at different polarities.

In section 4.3, we will show that by including a critical time loop (CTL) for minimizing the vacuum break or using an in-situ a-Si/TiN deposition process, the potential interfacial layer caused by (a) can be minimized (or fully avoided), leading to an improvement of MSM I-V symmetry. However, the asymmetry due to (b)-(c) can hardly be addressed at the moment, using the current test vehicle.

To summarize, we have experimentally proven that a doping-free thin silicon film MSM selector provides large non-linearity compared to the doped silicon devices with limited penalty on the drive current reduction. The results are consistent with the TCAD simulation prediction. In the next section, different approaches are evaluated aiming to further improve the device performance.

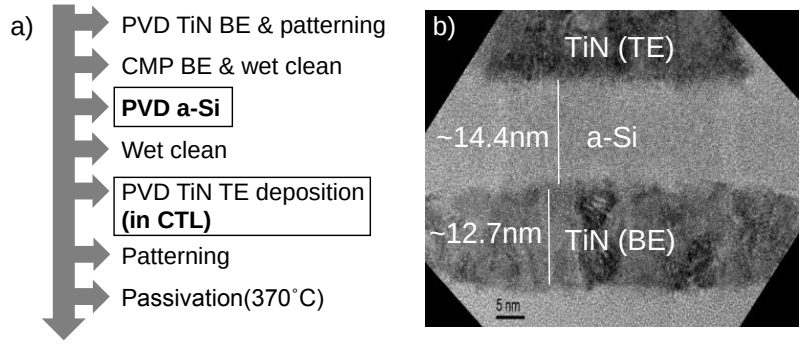


Figure 4.9: *(a) Process flow for PVD a-Si based MSM selector. The different process steps compared to the previous experiments are circled. (b) TEM picture for crossbar PVD 15nm a-Si MSM device. Cell Size: 40x40nm^2.*

4.3 MSM selector optimization

4.3.1 Impact of the a-Si thickness variation

4.3.1.1 Experiments

In the initial assessment, Silcore® technique was employed for Si deposition. Although conformal, this process requires thermal budget and long deposition time, being an unusual approach for silicon film deposition, which requires dedicated hardware configuration. In this part, we show that devices using conventional PVD amorphous silicon generate similar results. This implies that MSM is a robust concept, the highly non-linear and large drive current characteristics are reproducible for various a-Si deposition conditions.

The bottom and top TiN electrodes (BE/TE) and a thin amorphous-Si (a-Si) film were all deposited by room temperature sputtering (PVD). The target thickness of a-Si film was in a range from 8nm to 30nm. After a-Si surface wet cleaning, the TE was deposited subsequently in a critical time loop (CTL) for minimizing the formation of an interfacial layer, in contrast to the previous experiments (section 4.2.3) where CTL was not included. Fig.4.9.(right) shows TEM cross-section of a 15nm (target thickness) a-Si MSM structure. The microstructural analysis reveals the amorphous nature of the deposited Si layer after the passivation (370°C). The split table in this experiment is shown in TABLE.4.2.

Table 4.2: MSM devices split table (impact of a-Si thickness variation)

Splits	BE	Dielectric	TE	Doping(/cm^3)	Thermal budget (°C)
D1	TiN	8nm a-Si	TiN	undoped	370
D2	TiN	15nm a-Si	TiN	undoped	370
D3	TiN	30nm a-Si	TiN	undoped	370

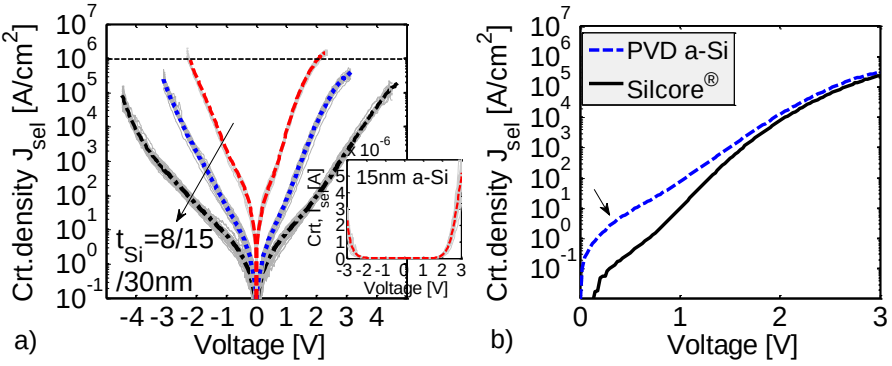


Figure 4.10: *(a) I-V plots for different silicon thickness devices. Inset: linear plot for 15nm a-Si thickness cells, showing rectification on both polarities. (b) I-V comparison of Silcore® and PVD a-Si MSM devices with the same target Si thickness of 15nm. Shoulder in the I-V characteristics of the PVD a-Si device is a typical fingerprint of trap-assisted tunnelling component. Cell size: 40x40nm^2.*

4.3.1.2 Results and discussion

Fig.4.10.(a) plots the I-V characteristics for devices with different PVD a-Si thicknesses. As compared to Fig.4.8, the symmetry is significantly improved with employing this CTL optimized process (Fig.4.10.a, inset), revealing the importance of top interface quality. Notice the I-V discrepancy between Silcore® and PVD a-Si, especially in the range of low bias (Fig.4.10.b). A shoulder in the I-V characteristics of the PVD a-Si device is a typical fingerprint of trap-assisted tunnelling (TAT) component, which strongly affects the leakage current at low bias. This I-V bump can be largely suppressed by applying a post-passivation annealing step, with the purpose of reducing the defect density in the as-deposited Si film. We will discuss further the impact of annealing in section 4.3.2.

Excellent I-V uniformity has been achieved across the 300mm wafer for devices down to 40x40nm^2 suggesting an excellent scalability of the MSM structure towards 10nm-size. With a dopant-free approach, a dopant activation anneal is no longer

needed, leaving the deposited Si film amorphous. Consequently, grain-size induced variability, specific to polycrystalline films, especially when device dimensions become comparable to the grain size, is expected to no longer be an issue. The current density at fixed voltage remains area-independent (Fig.4.11), proving that the current scales well with area.

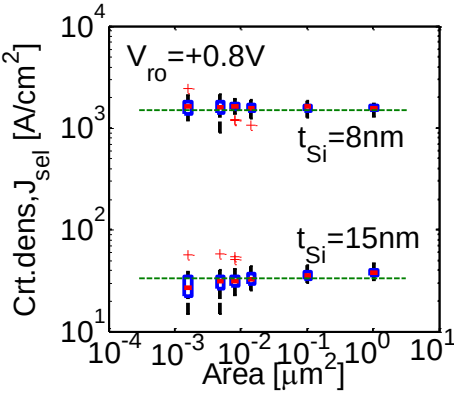


Figure 4.11: *Current density remains constant for devices of different size (40x40nm^2 to 1μm^2). The read-out current is sampled at +0.8V.*

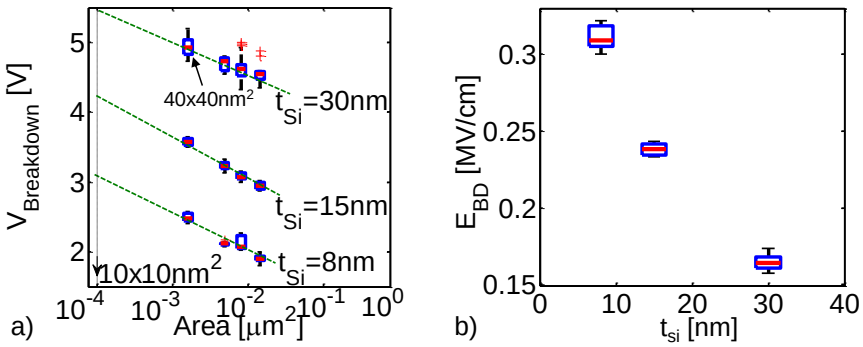


Figure 4.12: *(a) Extracted BD voltage for MSM devices with various a-Si film thicknesses. (b) Extracted BD field for various a-Si thicknesses (40x40nm^2).*

Fig.4.12.(a) extracts the breakdown (BD) voltages (e.g. for positive polarity) for devices with different cell sizes showing that V_{BD} increases with scaling, for any a-Si

thickness. For a given cell size, the BD field (E_{BD}) increases with reducing the a-Si thickness (Fig.4.12.b). As a consequence, the maximum drive current (J_{max}), which is limited by the BD voltage of the cell, is improved for thin a-Si thickness (Fig.4.13). The projected maximum current density J_{max} extrapolates towards 10^7A/cm^2, for a 10nm-size selector (Fig.4.13).

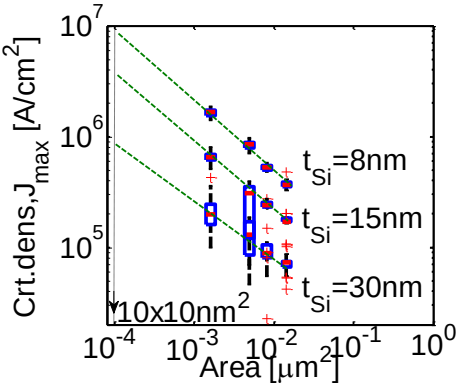


Figure 4.13: *Extrapolated maximum drive current density for MSM devices.*

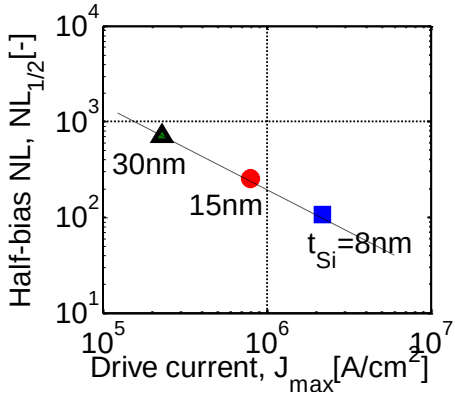


Figure 4.14: *A selector Figure-of-Merit NL½-J_{max} plot. NL½ is extracted at maximum current drive. Better J-NL trade-off is achieved by thickness-tuning effect. Cell size: 40x40nm^2.*

Fig.4.10, the 8nm a-Si MSM devices (40x40nm^2) show the best performance in

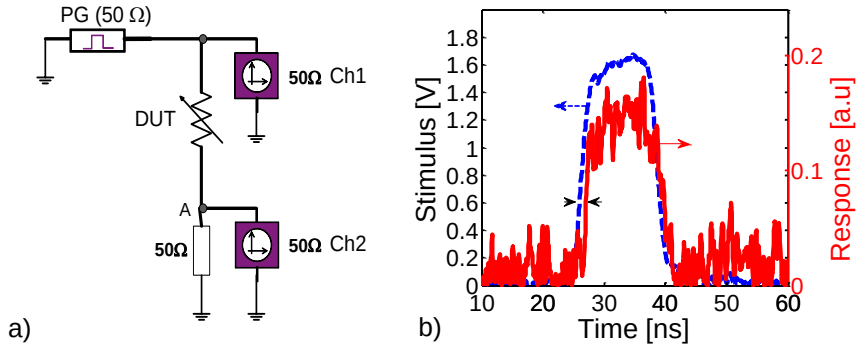


Figure 4.15: *(a) Scheme of the pulse measurement system. PG: pulse generator; DUT: device under test; CH: channel for oscilloscope (b) 10ns-pulse stimulus and collected response, showing fast turn-on and turn-off time (<1ns).*

terms of maximum drive current (limited by device breakdown) of about 2MA/cm^2 at 2.3V (reaches 1MA/cm^2 at ~2.0V) and a half-bias non-linearity NL½ of around 100. The latter is estimated as the current ratio between the maximum drive current (2MA/cm^2) and current at half of the voltage at which the drive current is achieved, i.e. NL½=J(V$_a$=2.3V)/J(V$_a$=1.15V), where V$_a$ is the applied voltage. With increasing Si thickness, larger voltages need to be applied in order to deliver the maximum drive current. If the half-bias non-linearity (NL½) and maximum drive current (J$_{max}$) are assumed as selector performance factors, a trade-off is observed for MSM devices (Fig.4.14). Reduction of a-Si thickness improves the maximum drive current, however, at the expense of decreasing NL½ as compared to the thick a-Si devices. A better J$_{max}$-NL½ trade-off is achieved for 15nm a-Si MSM. Note that the figures-of-merit in Fig.4.14 are extracted from MSM devices with 40x40nm^2. We expect that the drive current J$_{max}$ can be further improved with scaling, as suggested by the trend in Fig.4.13.

The MSM structure is expected to operate very fast, imposing no speed constraint on the full 1S1R cell. To confirm this, an input stimulus pulse voltage V$_{in}$=1.8V is applied to a 1μm^2 device, using the measurement setup schematically shown in Fig.4.15.(a). The recorded signal, collected on a small load resistance (50Ω) shows fast speed (<1ns), for both turn-on and turn-off times, Fig.4.15.(b). The fast switching is an intrinsic advantage of the junctionless structure, which eliminates issue related to the minority-carrier recombination/generation effects present in junction based (e.g. bipolar) diodes.

4.3.2 Impact of anneal

The proposed MSM structure has the advantage of using basic CMOS process steps, manageable thermal budget, and moreover, it is scaling friendly, projecting improved drive current towards 10nm-size. However, the non-linearity of the device needs to be improved to cut-off the leakage currents for enabling large 1S1R array size.

In this part, we present an optimized MSM structure by applying the anneal, leading to a device with improved performance such as high drive current exceeding 1MA/cm^2, and half-bias non-linearity of 1500.

4.3.2.1 Experiments

TABLE.4.3 summarizes annealing experiments for the MSM selectors. The reference splits, 8nm a-Si (D1) and 15nm a-Si (D5) devices are fabricated under the thermal budget of passivation (370°C). A post-passivation annealing (Fig.4.16.a) was applied at temperature ranging from 400°C to 500°C, for 5min time, for 8nm a-Si devices. A similar procedure was applied on the 15nm a-Si after the passivation (D7, D8), for up to 600°C, 5min. In order to evaluate the impact of annealing performed at different stages, a post-deposition anneal (PDA) was applied right after TE deposition (D9), Fig.4.16.b. The anneal was applied both before the TE stack etch and after passivation (D10). The TEM results for 600°C-annealed device (D8) shows limited morphological difference in the deposited Si layer after anneal, which remained amorphous (Fig.4.17.b).

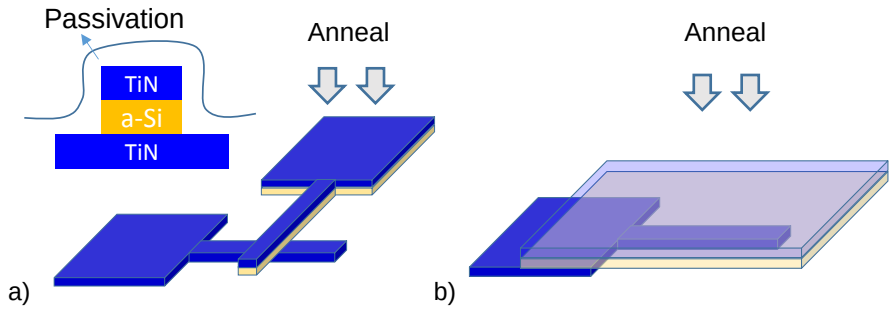


Figure 4.16: *(a) post-passivation annealing (PPA) (b) post-deposition annealing (PDA), before patterning.*

Table 4.3: MSM devices split table (impact of annealing)

Splits	BE	Dielectric (PVD)	TE	Anneal stage	Anneal temperature T(°C for 5mins)
D1	TiN	8nm a-Si	$TiN_{(in\_CTL)}$	N.A	N.A
D2-4	TiN	8nm a-Si	$TiN_{(in\_CTL)}$	PPA[a]	$400_{(D2)}$,$450_{(D3)}$,$500_{(D4)}$
D5	TiN	15nm a-Si	$TiN_{(in\_situ)}$	N.A	N.A
D6	TiN	15nm a-Si	$TiN_{(in\_CTL)}$	PPA	600
D7-8	TiN	15nm a-Si	$TiN_{(in\_situ)}$	PPA	$500_{(D7)}$,$600_{(D8)}$
D9	TiN	15nm a-Si	$TiN_{(in\_situ)}$	PDA[b]	600
D10	TiN	15nm a-Si	$TiN_{(in\_situ)}$	PDA+PPA	600 (5mins+5mins)

[a] Post-Passivation Anneal.
[b] Post-Deposition Anneal.

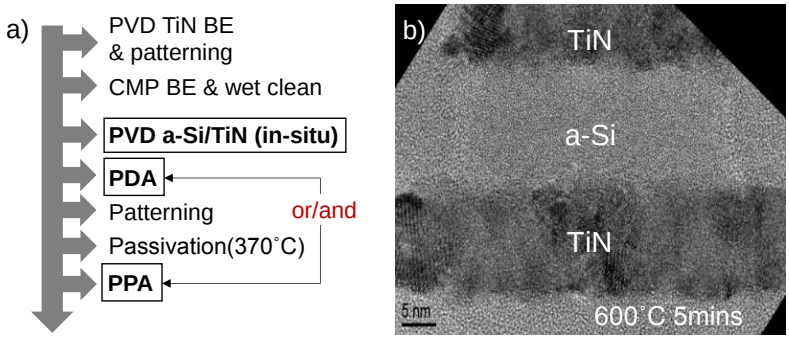


Figure 4.17: *(a) Process flow for crossbar MSM selectors, with a-Si/TiN (top electrode) in-situ deposition. (b) TEM results for 600°C-annealed structure, a-Si thickness: 15nm.*

Note that an in-situ PVD deposition of a-Si (15nm)/TiN top electrode was employed to further eliminate formation of thin interfacial oxides. However, the difference between the CTL and in-situ process is negligible, and can hardly be observed from the I-V characteristics.

4.3.2.2 Results and discussion

Fig.4.18 compares the I-V characteristics for the in-situ and ex-situ (with CTL) a-Si/TiN (top electrode) deposited MSM devices. Negligible difference of the I-V characteristics was observed after the anneal. This implies that the annealing process becomes the dominating control knob for tuning device performance.

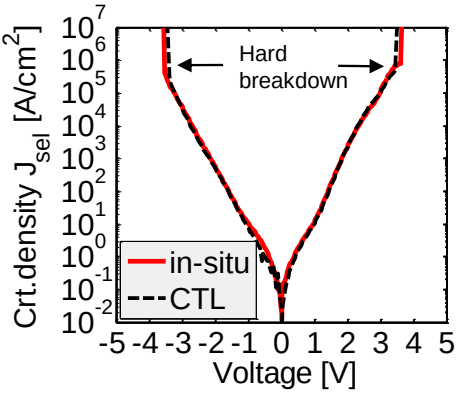


Figure 4.18: *I-V plots for 15nm a-Si thickness MSM devices with in-situ a-Si/TiN deposition (D8) and ex-situ a-Si/TiN process (D6) after post-passivation anneal at 600°C for 5mins. Data on 40nm-size devices.*

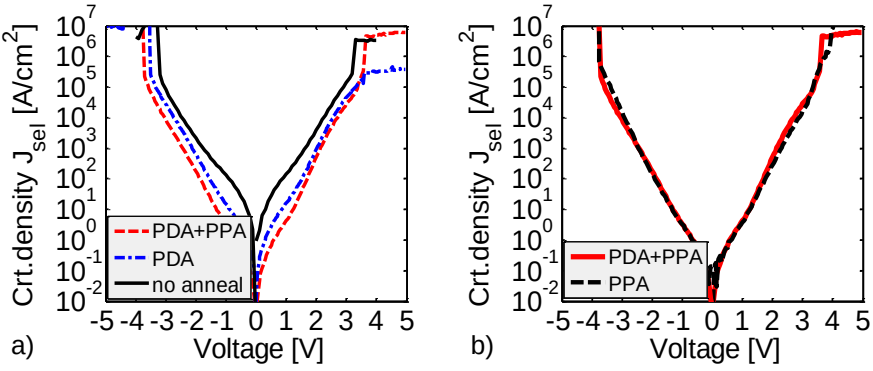


Figure 4.19: *I-V plots for 15nm a-Si thickness MSM device (a) unanneal; anneal after top electrode deposition (PDA); two-stage anneal including PDA and post-passivation anneal (PPA) (b) Comparison between D10: two-stage anneal and D8: post-passivation anneal only.*

a) Impact of the anneal stage

By performing the anneal directly after top electrode deposition (PDA) and just before etching, a reduction of leakage current compared to the unannealed device is observed. This happens especially at low bias where the I-V shoulder is suppressed, resulting

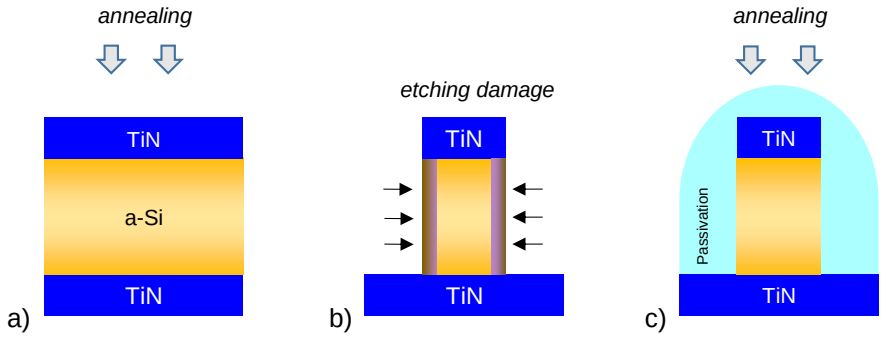


Figure 4.20: *Proposed model for explaining the impact of annealing stage. (a) annealing after TE deposition reduces the defect density in as-deposited Si film (b) etching damage on the sidewall (c) annealing after the passivation cures etching plasma damage.*

in an improvement in terms of non-linearity (Fig.4.19.a). This result suggests that a high temperature annealing could cure defects in as-deposited a-Si layer, and this reduces the trap-assisted tunnelling component. When an additional anneal step was applied on the same device after the passivation, a further reduction of low bias leakage current was observed (Fig.4.19.a). This implies that the improvement by anneal has two components: on the one hand, a high temperature anneal process after full stack deposition reduces the defect density in the a-Si layer (Fig.4.20.a). On the other hand, during pattering, a dry etch process may damage the sidewall of the cell (Fig.4.20.b), which provides additional leakage paths. With a thermal treatment after passivation, this plasma induced etch damage can be cured, leading to further improvement (Fig.4.20.c). To confirm this interpretation, we further compare the devices which being annealed twice (i.e. PDA + post passivation, 600°C/5min for each stage, total 10min) and devices which are annealed only once after the passivation at 600°C for 5min, Fig.4.19.(b). Negligible difference was found between them. Under a post-passivation anneal, both sidewall etching plasma damage and defects in the as-deposited Si layer can be cured at the same time. This comparison also suggests that the anneal time is not a critical control parameter for determining the device I-V characteristics.

b) Impact of anneal temperature

In this part, we further evaluate the impact of the annealing temperature. Post-passivation anneal was applied, with a duration of 5mins.

I-V characteristics for devices with different a-Si thickness show that a 5min annealing for up to 600°C after passivation improves the non-linearity without affecting the

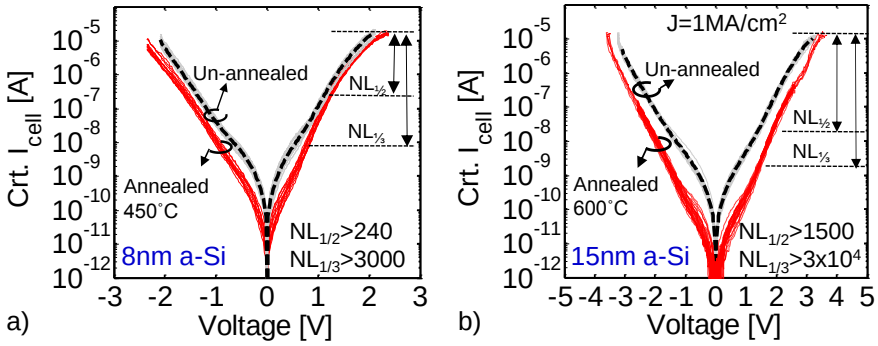


Figure 4.21: *I-V plots for (a) 8nm and (b) 15nm a-Si thickness, MSM devices before and after post passivation annealing. Data on 40nm-size devices.*

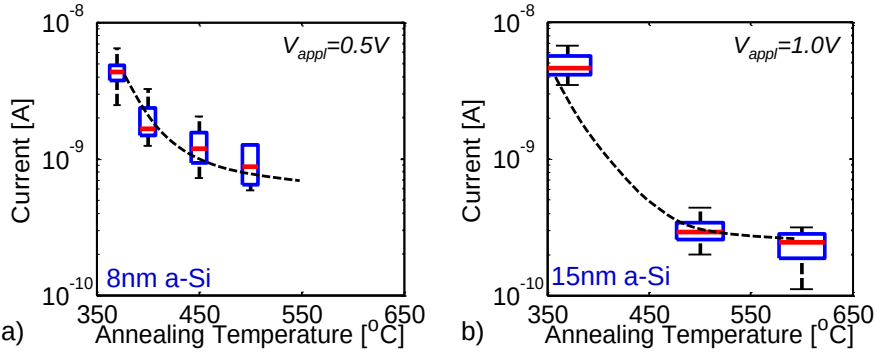


Figure 4.22: *Leakage current at low bias 0.5V for 8nm (a) and (b) at 1.0V bias for 15nm a-Si MSM selectors for different anneal temperatures (anneal time was 5min). Device size: 40x40nm^2.*

maximum drive current, at any a-Si layer thickness (Fig.4.21). High current density of over 10^6A/cm^2 at 3.6V and half-bias non-linearity (NL½) of about 1500 are achieved for 15nm a-Si annealed devices on 40x40nm^2 cell size (Fig.4.21.b). For thin 8nm a-Si device, the anneal effect is clearly visible after a thermal budget of only 450°C. The annealed devices (40x40nm^2) achieve a maximum drive current of over 10^6A/cm^2 at 2.6V with a NL½ of about 240 (Fig.4.21.a).

The low bias leakage improvement increases with the annealing temperature (Fig.4.22), with a tendency to saturate at about 500°C, for any a-Si thickness. This decrease of low

bias leakage current leads to non-linearity improvement. For thicker 15nm a-Si MSM, a larger decrease of low bias leakage is achieved compared to thin 8nm-Si devices, which leads to stronger non-linearity improvement.

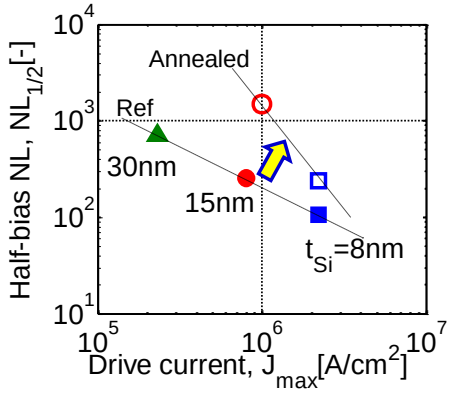


Figure 4.23: *A selector Figure-of-Merit NL½-J_{max} plot. Significant NL improvement and better J-NL trade-off are achieved by combined anneal-thickness effect. NL½ is extracted at maximum current drive. Cell size: 40x40nm^2.*

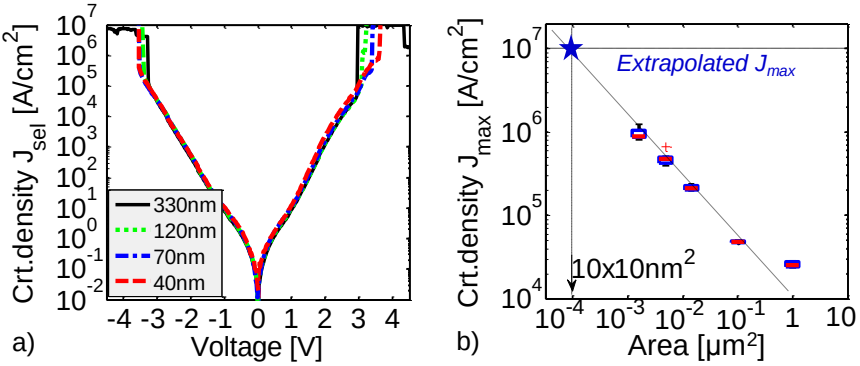


Figure 4.24: *(a) I-V plots for 15nm a-Si thickness annealed (600°C 5mins post-passivation annealing) MSM devices with various area. (b) The estimated J_{max} exceeds 10MA/cm2 at 10x10nm^2, J_{max} is limited by the breakdown voltage.*

Although the annealing process improves both 8nm and 15nm a-Si MSM devices, significant non-linearity improvement and better J_{max}-NL½ trade-offs are achieved

for the thicker 15nm a-Si device (Fig.4.23). Besides a stronger reduction of low bias leakage current, 15nm a-Si devices display a larger voltage operation range (e.g. 3.6V), which further improves the half-bias NL½, compared to thin 8nm devices (e.g. 2.4V). Moreover, a large voltage operation range improves the 1S1R cell nonlinearity, especially for the write operation, as discussed in the previous Chapter 3.

Selector performance for the annealed MSM devices is projected to improve by scaling, similar to the unannealed MSM devices (Fig.4.12). The breakdown (BD) voltage increases with decreasing cell size (Fig.4.24.a), which improves the maximum current density (J_{max}). For 15nm a-Si devices, the J_{max} is extrapolated towards 10MA/cm^2 (Fig.4.24.b), which enables 10µA switching current for a 10nm-size resistive switching element (RSE) structure. This may relax the requirement on the maximum switching current the selector is able to withstand.

c) Understanding

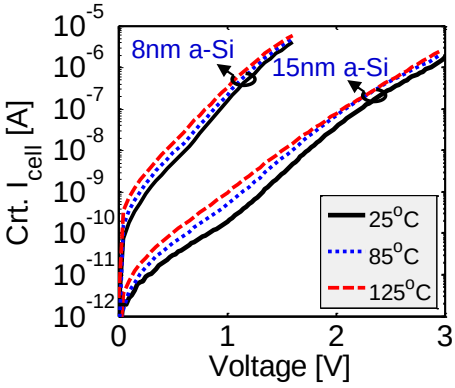


Figure 4.25: *Temperature dependent I-V characteristics for 8nm and 15nm a-Si devices (unannealed), evidencing stronger I(T) variation in the low-bias range, for both splits.*

To confirm the underlying conduction mechanism and the improvement by annealing, temperature dependent measurements were done on the MSM devices. Selector I-Vs show a weak temperature dependence at high bias, which is consistent with a tunnelling-based dominant conduction mechanism (Fig.4.25). Furthermore, temperature dependence is stronger at low bias and slightly increases with a-Si thickness, indicating a different dominant conduction mechanism. As mentioned before, the shoulder (e.g. bump in the I-V characteristic) at low bias [156–160] indicates that trap-assisted tunneling (TAT) is the dominant conduction mechanism.

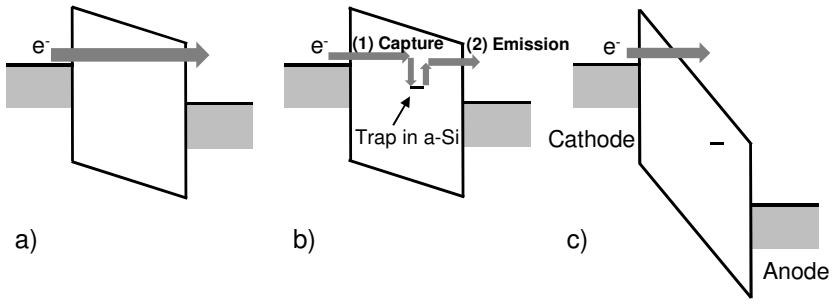


Figure 4.26: *Schematic of process (a) defect-free direct tunnelling (b) trap-assisted tunnelling (c) FN tunnelling.*

The defect-free tunnelling current through the energy barrier depends, to the first order estimation, exponentially on the barrier shape (e.g. height, width), which electron have to tunnel through (Fig.4.26.a). Traps in the a-Si layer are acting as stepping-stones, which allow electrons to tunnel through thinner barriers, increasing the number of conductive channels for the electron flow. The increase of total current is prominent in the direct tunnelling (DT) regime at a small bias (Fig.4.26.b), which contributes to the low bias I-V shoulder. When a large voltage is applied (e.g. at high field), the device enters the Fowler-Nordheim (FN) region where the electron tunnels through a triangular energy barrier directly to the conduction band of a-Si, and then flow to the anode (Fig.4.26.c), without interacting with traps. In this case, the TAT current component becomes negligible and the leakage current is dominated by the FN tunnelling current. The TAT current, which depends on the trap depth and density, may have a stronger temperature dependency, depending on trap depth and the strength of the electron-phonon interaction [161, 162] . This is in line with our observation in Fig.4.25.

A trap-assisted tunnelling (TAT) model [163] is able to explain the low-bias I-V characteristics for both annealed and unannealed samples (Fig.4.27). The TAT model fits experimental data well, in the low bias region, with the same set of parameters, except for the extracted trap density, which decreased by a factor of ~5 by annealing. Furthermore, at higher biases, a defect-free tunnelling model [164] explains the experimental data, for both annealed and unannealed samples.

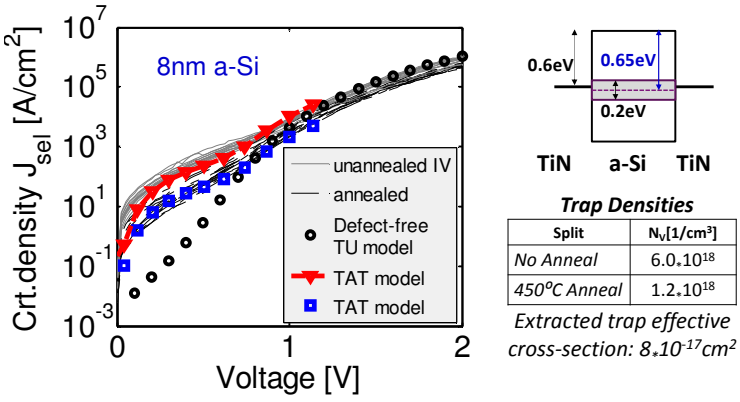


Figure 4.27: *(left): TAT (low-bias) [163] and defect-free tunnelling (TU) (high bias) [164] conduction models explain experimental IV's for both 450°C-annealed and un-annealed samples. (right): The MSM band diagram, with a 0.65±0.1eV extracted narrow trap band and bulk trap densities corresponding to the 2 splits.*

4.3.3 Impact of barrier engineering

In section 4.2.2, we have shown the trade-offs for achieving both high drive current and large non-linearity at the same time for a single a-Si layer MSM selector. The device performance mainly depends on two parameters [165]: M/S barrier height (ϕ_b) and thickness of a-Si (t_{Si}). By reducing the ϕ_b and t_{Si}, the electron tunnelling probability increases, and so does the current. However, this comes at the cost of losing the non-linearity, as the device becomes more leaky throughout the whole bias range. On the contrary, increase of the barrier height and a-Si thickness improves non-linearity, however, it reduces the drive current.

To bypass this performance trade-off, we can try to decouple control knobs of the drive current and of the non-linearity, by placing an additional material with larger barrier height than that of a-Si in the middle of the original MSM structure (Fig.4.28). By doing this, at low bias, the current flowing through the cell can be further suppressed due to the presence of the additional barrier seen by the tunnelling electrons (Fig.4.28.e). When high bias is applied, the impact of the middle layer is minimized due to the barrier lowering. Thus, the maximum drive current is mainly controlled by ϕ_{b1}, which is mostly determined by the M/a-Si interface. This triple-layer selector is introduced as Thin-Silicon Injector (TSI) [165], which has a simple M/S/I/S/M structure with 'I' as middle barrier, 'S' as the a-Si.

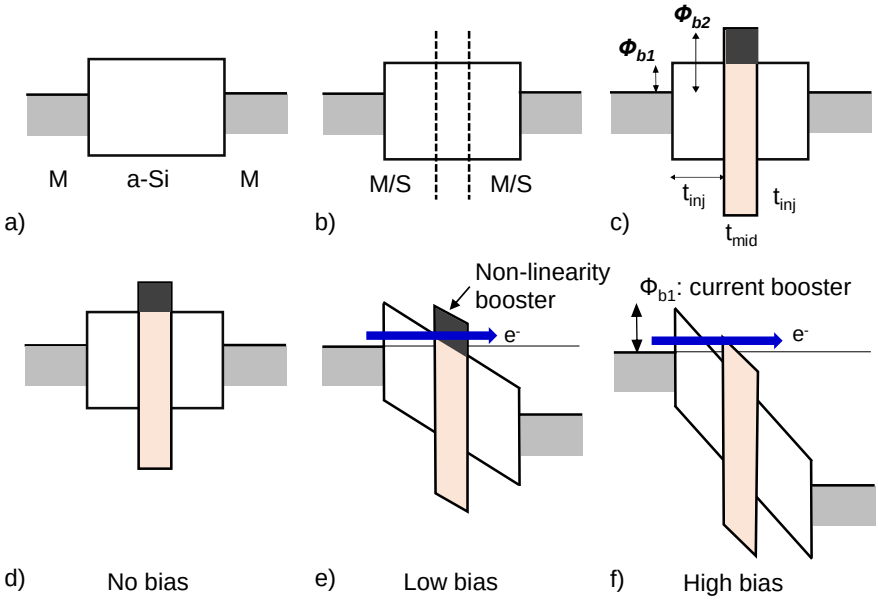


Figure 4.28: *(a)-(c): Principle of Thin-Silicon Injector (TSI). Additional layer is inserted in the middle with barrier height ϕ_{b2} larger than ϕ_{b1} of single layer MSM device. (d)-(e): the tunnelling probability (current) is suppressed due to the additional barrier at low bias, results in non-linearity improvement. (f): large applied voltage suppresses the middle barrier, the maximum drive current is mainly controlled by the M/S interface. Adapted from [165].*

a) Experiments

The crossbar test vehicle was employed for fabricating the TSI selectors. After CMP planarization of the bottom electrode (TiN), the full selector stack (including the TiN top electrode) was formed by an in-situ PVD process, followed by the patterning and passivation. A final thermal anneal at 600°C for 5mins was applied after passivation, aiming to reduce defect density for the as-deposited films. A modification of the a-Si deposition was included, which allows deposition of SiN_x with tuning of Nitrogen content (%) during a-Si sputtering, by controlling the N_2 gas flow in the PVD chamber [165]. In this way, the full stack, i.e. a-Si/SiN_x/a-Si/TiN(TE) is formed in an in-situ process, which avoids interface layer formation in the device. TABLE.4.4 summarizes the TSI selector experiments.

With the current TSI selector design, we expect the proposed selectors have a similar high drive current with respect to the original MSM device, but with an improved

Table 4.4: TSI devices split table

Splits	BE	Dielectric	TE
D1	TiN	8nm a-Si$_{(reference)}$	TiN$_{(in_situ)}$
D2	TiN	8nm SiN$_{28\%}$	TiN$_{(in_situ)}$
D3	TiN	4nm a-Si/4nm SiN$_{28\%}$/4nm a-Si	TiN$_{(in_situ)}$
D4	TiN	4nm a-Si/4nm SiN$_{49\%}$/4nm a-Si	TiN$_{(in_situ)}$
D5	TiN	4nm a-Si/8nm SiN$_{28\%}$/4nm a-Si	TiN$_{(in_situ)}$
D6	TiN	6nm a-Si/4nm SiN$_{28\%}$/6nm a-Si	TiN$_{(in_situ)}$

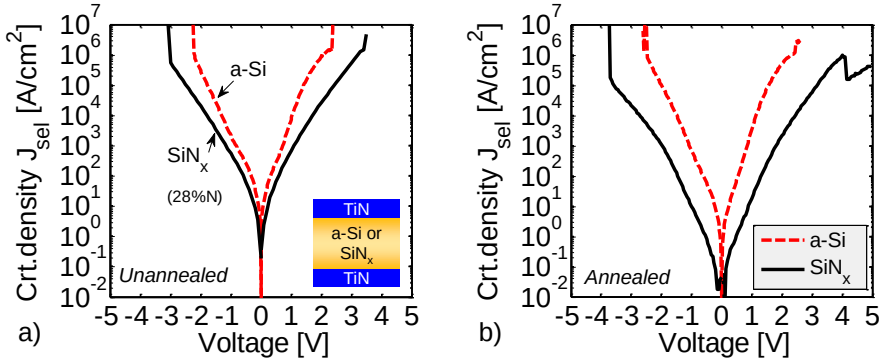


Figure 4.29: *(a) I-V plot for unannealed MSM device with 8nm a-Si and 8nm SiN$_x$.(b) I-V characteristics after post-passivation anneal at 600°C for 5mins, for both devices. Data on 40x40nm^2 devices.*

non-linear characteristics.

b) Results and discussion

To confirm the impact of Nitrogen for barrier height tuning in a-Si dielectric layer, MSM with single layer SiN$_{28\%}$ (D2) is compared to the reference a-Si based device (D1). Fig.4.29.(a) shows that the current decreases for SiN$_x$ based device, which is consistent with a barrier height/bandgap increasing due to the presence of Nitrogen in Silicon. However, the difference between the two I-V curves is small at low bias. This can be related to a large trap density in the as-deposited SiN$_x$ film. When a post-passivation anneal is applied, leakage current is strongly reduced (Fig.4.29.b), thanks to the reduction of trap density in the SiN$_x$ film and the recovery of the sidewall plasma damage, similar to the effect that has been observed for a-Si based MSM as we discussed before.

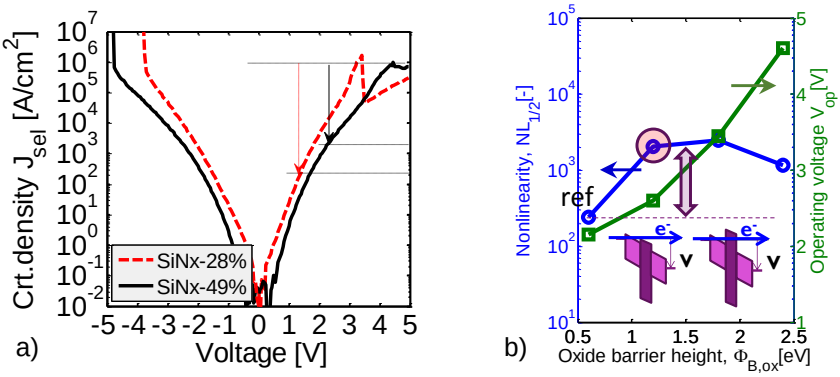


Figure 4.30: *(a) The impact of increasing N concentration in TSI stack 4nm a-Si/4nm SiN_x/4nm a-Si. The stack is annealed at 600° for 5mins. Data on 40x40nm^2 devices. (b) Predicted impact of inner barrier height by [164].*

The triple layer TSI selector, e.g. 4nm a-Si/4nm $SiN_{28\%}$/4nm a-Si (4/4/4), shows half-bias non-linearity (NL½) of about 1600, the maximum current density over 1MA/cm^2 (Fig.4.30.a). Increasing the Nitrogen content (e.g. N:49%) in the inner SiN_x layer would increase the bandgap of the material, the leakage current decreases over the whole bias range as compared to lower N% content devices (Fig.4.30.a). However, this leads to a saturation of the non-linearity gain and eventually the NL½ starts decreasing. This is due to a too high barrier of SiN_x, which can hardly be made "invisible" by applying high voltage. Indeed, such trend is in line with the simulation calculation (Fig.4.30.b), where the NL½ and operating voltage are extracted from the simulated I-V characteristics for TSI structures, using the model described in [164] (assuming defect-free tunnelling). The operating voltage (V_{op}) is the voltage at which current density reaches 1MA/cm^2, NL½ is defined as the ratio between current at V_{op} and the current when the selector is biased at ½V_{op}, oxide barrier height ϕ_{ox} (ϕ_{b2}) is considered as the inner barrier height, and the 'ref' is the estimated barrier height at the TiN/a-Si interface (e.g. 0.6eV). As can be seen, an optimal ϕ_{b2} ranging from 1.2eV to 1.8eV provides the best NL½. The NL½ decreases when the inner barrier ϕ_{b2} is beyond the optimal range.

Finally, the best TSI selector NL½ is improved towards 6400 (Fig.4.31) when thicker (8nm) SiN_x is employed. This TSI device 4nm a-Si/8nm $SiN_{28\%}$/4nm a-Si (4/8/4) has similar total stack thickness compared to original single layer 15nm a-Si MSM. However, it provides much larger non-linear characteristics. These results confirm the feasibility for achieving higher NL½ by adjusting the barrier profile for a-Si based tunnelling selector.

We have noticed that trap-assisted tunnelling (TAT) mechanism remains an important

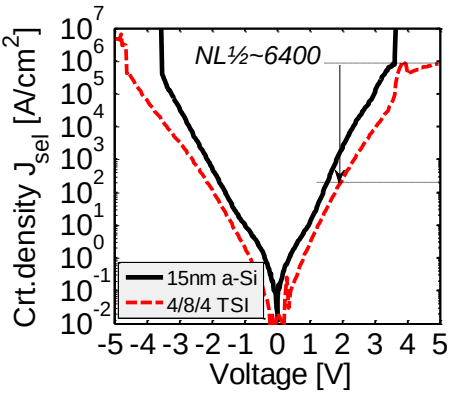


Figure 4.31: *I-V characteristics of TSI stack with 4nm a-Si/8nm $SiN_{28\%}$/4nm a-Si. The non-linearity is improved compared to original single layer MSM selector of similar stack thickness (~15nm). Both devices are annealed at 600°C for 5mins. Data on 40x40nm^2 devices.*

non-linearity degradation mode, as TAT facilitates large leakage current at low biases. The defect density, however, can be lowered by applying additional thermal anneal. The post-passivation is an efficient way for improving both single-layer MSM and triple layer TSI structures.

4.3.4 Summary

Selector performance requirements are multiple, e.g. the required current density comes from device constraints (e.g. SET/RESET current), non-linearity and voltage compatibility are mainly derived from the aspects of circuit performance, as we already discussed in Chapter 3. Here, we simply assume the maximum drive current density (J_{max}) and half-bias non-linearity (NL½) as the figures-of-merit for benchmarking of a-Si based tunnelling selectors (Fig.4.32).

Considering cross-point array of 1Mbit size with 1μA resistive switching element (RSE) at 10nm-scale, the minimal required selector NL½ is extrapolated towards 800 (Section 3.3.3). The annealed 15nm layer a-Si MSM and all proposed TSI selectors meet this requirement. Moreover, the proposed a-Si based selectors have sufficient operating voltage range, which is compatible with typical HfO_x based resistive memory [17, 126] with program voltage of about ±1.5V.

When a RSE with large switching current is assumed (e.g.10μA), NL½-J_{max}

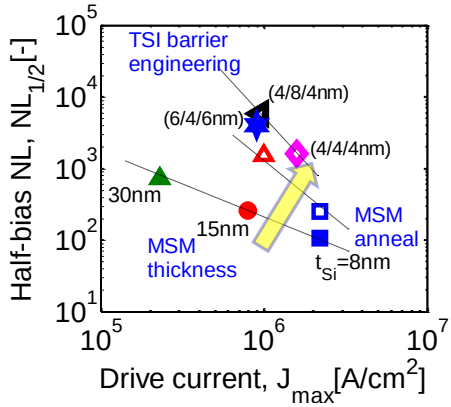


Figure 4.32: *NL½ and maximum drive current plot for annealed TSI selector, with single-layer MSM selectors. Data on: 40x40nm^2 device.*

requirements for a selector extend to NL½>2000 and J_{max}>10^7A/cm^2 (Section 3.3.3) targeting scalability of the resistive element to 10nm. In this case, the drive current density becomes a big challenge for the proposed a-Si based selectors. For the TSI structure, the maximum drive current depends mostly on the barrier height of the M/a-Si interface while to a second order dependency of the inner layer barrier height. Thus, the drive current is potentially improved by reducing barrier height, e.g. with low workfuntion metal. Moreover, it is expected that scaling of the devices towards small cell size can allow improvement on current drive by extending the breakdown voltage. Nevertheless, the current deliverability of the a-Si based selector towards 10nm-scale remains subject of further investigation. Considering the worst case (i.e. J_{max}~1MA/cm^2), the device dimension has to be relaxed (e.g. ~30x30nm^2) in order to enable a 10μA switching RSE. This is not suitable for mass data storage memory application (e.g. replacing post-NAND technology), as it requires extremely high area efficiency. One the other hand, 1S1R cross-point arrays with a-Si based selectors may be suitable for the potential Storage Class Memory (SCM) [28], of which memory device requirements fall in between high performance memory (e.g. cost/area efficiency insensitive) and low-cost storage-type memory (e.g. NAND).

Finally, benchmarking of literature reported (type-I) selector structures is summarized in Fig.4.33. To achieve promising performance while fabricating in a CMOS-compatible process using fab-friendly materials, remains a challenge for the selector device implementation. Selectors reported in [94] show excellent performance, however, they are not integratable due to the adoption of Pt electrodes. While other issues, e.g. voltage compatibility, reliability remain problems for [112]. These factors should be considered as equally important performance indicators, next to the NL½

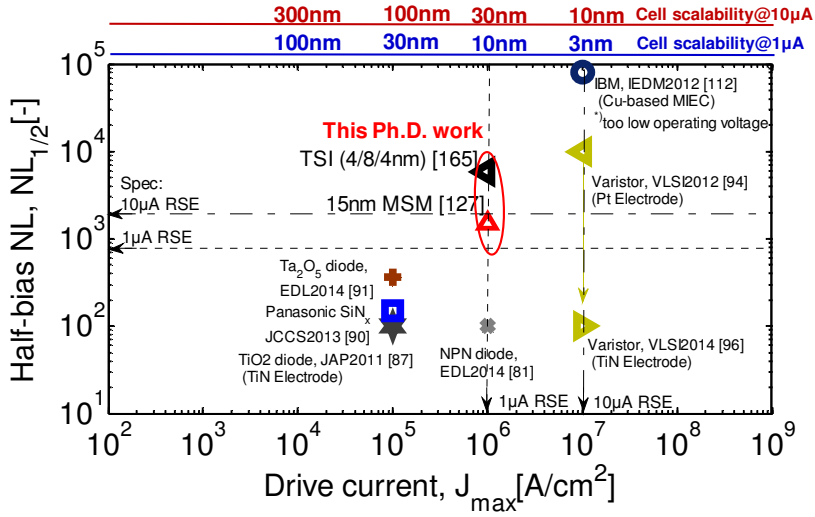


Figure 4.33: *Selector benchmark [81, 87, 90, 91, 94, 96, 112, 127, 165].*

and maximum drive current (J_{max}) when designing selector device.

4.4 Reliability

In this part, we investigate the reliability of the proposed a-Si based MSM devices. The selector suffers voltage stress during the memory operation of 1S1R devices, especially during the write operation when high program voltage is involved. Preliminary AC pulse stress of $\pm$2.2V/10ns on the 8nm a-Si unannealed MSM devices leads to progressive increase of the leakage current at low bias, over an endurance test of 10^9 cycles (Fig.4.34). This is a typical signature for defects generated in the a-Si during the electrical stress, which enhances trap-assisted tunnelling current, dominating the current conduction in the low bias range (Fig.4.34.a). Such wearing-out phenomena is similar to that of Stress Induced Leakage Current (SILC) [156–160] common for the degradation of the tunnel oxide in Flash memory cells.

4.4.1 DC stress

To investigate the MSM degradation, DC Constant Current Stress (CCS) measurement is performed on the 8nm a-Si MSM crossbar selector, where the schematic of the test

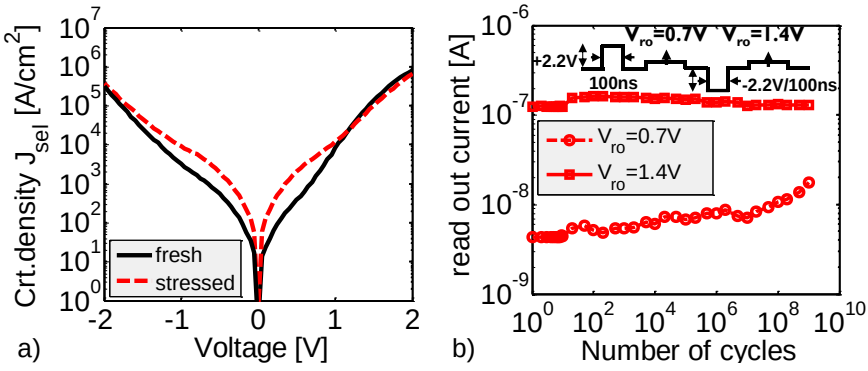


Figure 4.34: *(a) I-V characteristics of 8nm a-Si MSM (unannealed) before and after AC cycling stress. (b) The monitored readout current at +0.7V and +1.4V. Test done on cell with size: 40x40nm^2.*

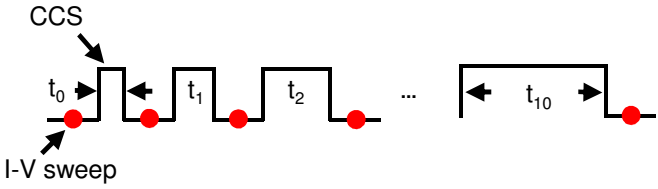


Figure 4.35: *Measure-Stress-Measure test plan for CCS measurements on 8nm a-Si unannealed MSM selectors.*

flow is shown in Fig.4.35. After an initial I-V sweep on the fresh cell, CCS at a fixed stress current density (J_{stress}) was applied. Each stress period lasts for t_i (i=0,1,2..) second(s) and then it stops, followed by a I-V sweep. Such measure-stress-measure loop continues till accumulated stress time reaches ~1024s. The discrete stress period, e.g. t_0,t_1,..t_{10} equals to 1s, 2s, 4s, 8s, ..512s, respectively. Note that t_0=1s is the minimal stress time in this experiment. During each I-V sweep, the stop voltage is limited at 1.5V to avoid additional degradation during the cell readout, i.e. the degradation is purely caused by the CCS.

Fig.4.36 shows the selector leakage current before and after a CCS of $2.5*10^6$A/cm^2 (J_{stress}) for two different levels of the injected charge fluence (Q_{inj}), i.e. 10^8A/cm^2 and $3*10^6$A/cm^2, Q_{inj} corresponds to the product of J_{stress} and accumulated CCS stress time. The post-stress I-V (dash line) suggests two effects: firstly, for the same stress current density (J_{stress}), the leakage current increases with the injected charge

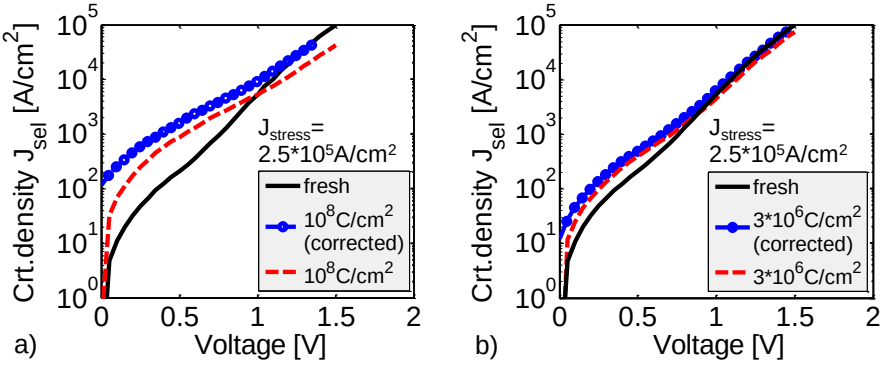


Figure 4.36: *(a) Measured selector I-V characteristics on 8nm a-Si MSM before and after CCS stress of J_{stress}=2.5∗10^{6}A/cm^2 for injected charge fluence (Q_{inj}=J_{stress}∗accumulated stress time)=10^{8}C/cm^2. (b) Q_{inj}=3∗10^{6}A/cm^2. Dash line: after stress. Circle: after correction for charge trapping. Data on cell size: 60x60cm^2.*

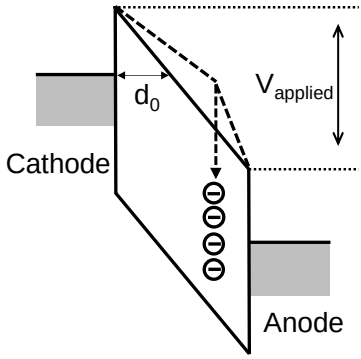


Figure 4.37: *The effective barrier width increases due to negative charge trapping in a-Si compared to d_0 in the charge-free scenario.*

fluence (Q_{inj}). Secondly, a horizontal post-stress I-V shift at large bias can be caused by charge trapping, e.g. negative charge in a-Si (Fig.4.37) during the stress, which increases the effective barrier width for electrons tunnelling through, thus reducing the current. To eliminate the latter effect for allowing a comparison between the fresh and degraded device under the same cathode field [160], a correction is included in the stressed I-V by adding the voltage shift ΔV as function of Q_{inj}. After correction, the I-V curve (circled) for the degrade device is identical to that of fresh device at high bias.

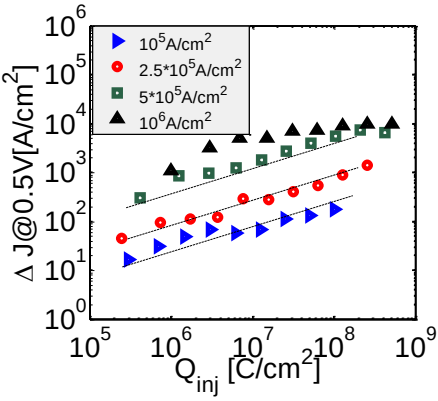


Figure 4.38: ΔJ *versus injected charge fluence* (Q_{inj}) *for different* J_{stress} *conditions. Data on cell size: 60x60cm*^{2}.

The increase of leakage current (ΔJ) can be extracted by subtracting the initial I-V from the corrected I-V after each stress period. ΔJ at fixed readout voltage of +0.5V (E_{field}~6MV/cm) is plotted in Fig.4.38, versus Q_{inj} for different CCS stress current density ranging from J_{stress}=10^5A/cm^2 to 10^6A/cm^2. A power law dependence of ΔJ on both J_{stress} and Q_{inj} is observed following,

$$\Delta J \sim Q_{inj}^{0.4} \cdot J_{stress}^{0.6} \tag{4.3}$$

Where 0.4 and 0.6 are the extracted fitting numbers. A similar quantitative model has been used for describing SILC in the MOS structures, where the increase of the leakage current can be modeled by a power dependency of the injected charge influence and the stress current, which has a one-to-one correlation with oxide trap generation [160]. Based on the current experimental observation, we believe that trap generation in the a-Si layer also plays a crucial role in the degradation for the MSM devices.

During the stress, an increasing number of the generated traps through the dielectric layer may ultimately cause breakdown of the material, i.e. time dependent dielectric breakdown (TDDB). However, this failure was not observed for MSM selector during CCS stress, possible due to a limited total stress time.

The degradation of MSM is found to be recoverable after anneal (Fig.4.39.a). In the experiment, the devices have been stressed at room temperature (CCS). The read-out current increases after the stress, Fig.4.39.(a), left part. Then the devices were baked at 250°C in air ambient. The leakage current was measured at room temperature after each baking period, e.g. 100s, 1000s and after 2hrs, Fig.4.39.(a), right part. As can be seen, the degradation is largely cured by the baking process. The extracted 'time-to-recovery',

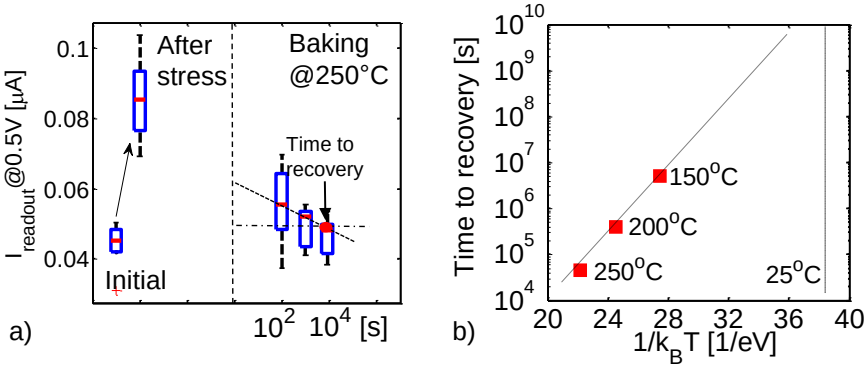


Figure 4.39: *(a) Time evolution of readout current with baking time at 250°C. The degradation (i.e. increasing of readout current) is generated by applying CCS at 2.5*10^5 for 1000s at room temperature. (b) Activation energy extrapolation for defect removal process.*

e.g. anneal time to fully recover the device to the initial characteristics (Fig.4.39.a, right-hand), is extrapolated to be around 4.5*10^{4}s at 250°C. Using the same approach, the 'time-to-recovery' has been extracted for different anneal temperatures (Fig.4.40.b). The activation energy for the recovery process is determined to be E_a~0.9eV. This E_a value is found similar to the energy barrier for defect creation in a-Si [166], where the barrier is associated with Si-Si bond breaking. Thus, we expect the MSM degradation is due to the Si-Si bond breaking created by electrical bias stress, and these defects can be removed by annealing which in turn brings devices to their initial behavior. However, the estimated time-to-recovery is over 10^{10} at room temperature (25°C), and ~3*10^8 at 85°C. Thus, such increase of low bias leakage for MSM selector can be considered as permanent degradation at operating conditions.

4.4.2 AC stress

So far, we have analyzed the MSM reliability under DC stress condition. In the following part, AC stress experiments are discussed. Both unipolar and bipolar stress are carried out showing similar degradation behavior compared to that under DC stress.

Firstly, unipolar AC stress with different pulse widths (e.g. 100μs, 10μs and 100ns) were employed. For a given device, a certain pulse duration is selected and pulse amplitude is fixed to +2V, at which voltage the device provides the target drive current (~1MA/cm^2). A readout voltage at +0.5V/100μs is applied after each pulse stress. The ratio between the read-out current ($I_{readout}$) and the initial $I_{readout}$ (I_0) for the fresh

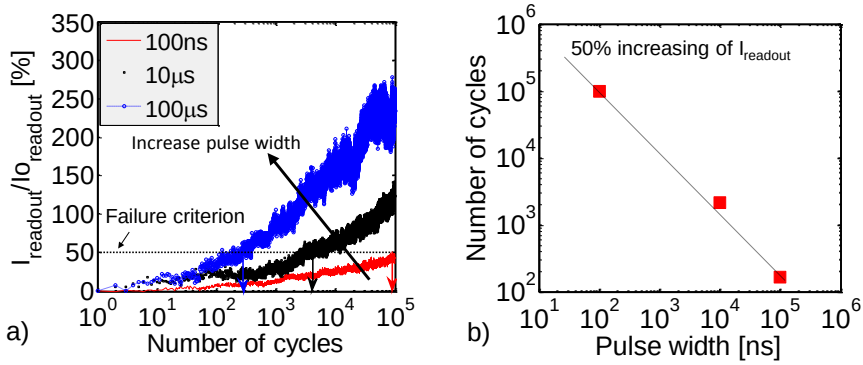


Figure 4.40: *(a) Percentage change of readout current at +0.5V versus number of cycles for different pulse width stress (b) Extracted maximum number of cycles (reaching the failure criterion)versus pulse width. Cell size: 40x40nm^2.*

device is considered as the figures-of-merit for monitoring degradation, which value is recorded after each pulse stress (Fig.4.40.a). If a failure criterion of 50% increase of $I_{readout}/I_0$ is assumed, it is found that the device fails much faster for large pulse duration, compared to using short pulse widths. The extracted maximum number of cycles under the failure criterion (50% shift of $I_{readout}$) follows a linear relationship with pulse width (Fig.4.40.b). This is in line with the previous DC stress results, indicating that degradation is cumulative by the total charge injected to the device. Thus, a short pulse operation is desired for MSM selector, as it allows large endurance cycles (i.e. to delay the degradation, relative to the number of cycles it withstands).

According to the pulse waveform extracted from the oscilloscope, the correspond current (J_{pulse}) flowing through the device is estimated under the DC I-V characteristic look-up table, e.g. assuming that selector has same DC and AC pulse I-V behavior. Thus, by computing the integral of J_{pulse} and time, the Q_{inj} injected to the device during a single pulse stress can be obtained (Fig.4.41.a). Finally, the shift of readout current can be re-plotted as a function of injected charge fluence Q_{inj} (Fig.4.41.b), the projected lifetime is estimated at ~$4*10^4$C/cm^2 for the MSM device under program stress (1MA/cm^2) condition.

To mimic practical memory operation, bipolar pulses were applied on the TSI devices (Fig.4.42). The results show marginal degradation after 10^5 cycles under bipolar pulse stress of 100ns duration. The pulse amplitude is set at the voltage that provides the maximum drive current. After 10^7 cycles, strong increase of the read-out current at low voltage is observed. The I-V before and after stress (Fig.4.42.b) suggests similar degradation mode for TSI device compared with purely a-Si based structure. Similar degradation occurs for thick 15nm a-Si MSM (annealed) devices (Fig.4.43).

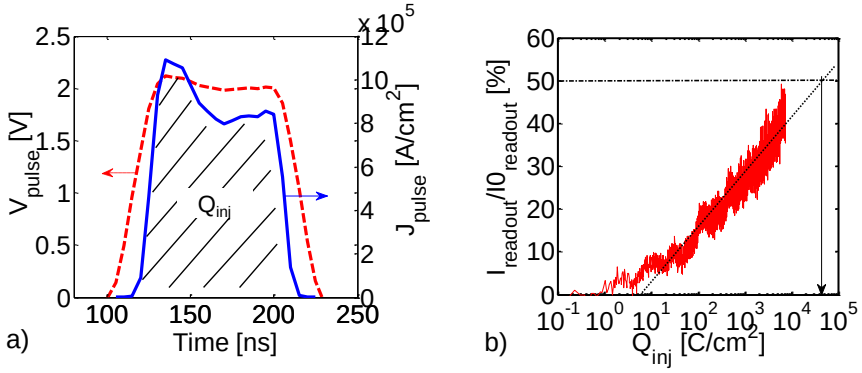


Figure 4.41: *(a) Estimation of pulse current according to AC pulse voltage (b) Percentage change of readout current versus the injected charge fluence. Cell size: 40x40nm^2.*

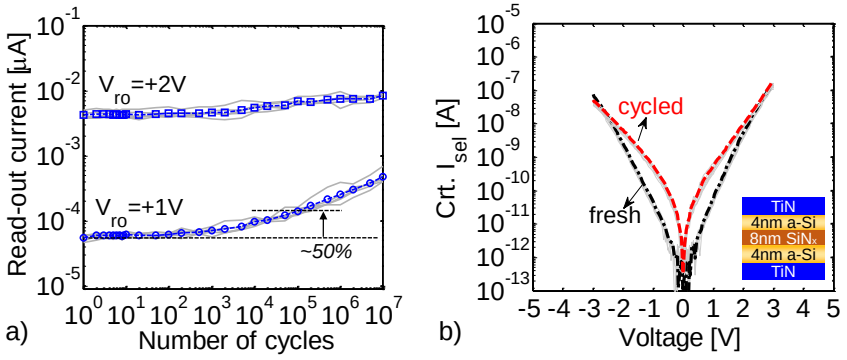


Figure 4.42: *Bipolar stress on TSI selector. (a) AC cycling of bipolar pulses ±3.8V/100ns, voltage of reaching maximum drive current (Fig.4.32). The readout voltage are set at +2V and +1V. (b) DC I-V characteristics before and after AC cycling after 10M cycles. Cell size: 40x40nm^2.*

4.4.3 Thermal stability

The MSM selector has excellent thermal stability. For instance, the 15nm a-Si MSM (annealed) show excellent stability under thermal stress (Fig.4.44). Baking test at 125°C

for 3 hours shows no degradation of cell characteristics, indicating that temperature has a limited impact on the device performance.

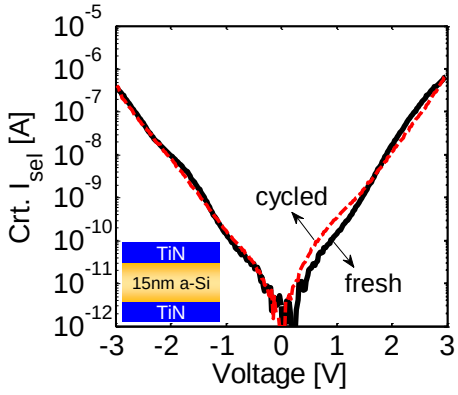


Figure 4.43: *Bipolar pulse stress on 15nm a-Si MSM selectors. Comparison of the I-V characteristics before and after electrical stress, showing limited degradation at any bias point. Stress condition: ±3.6V/100ns for 10^6 cycles. Cell size: 40x40nm^2.*

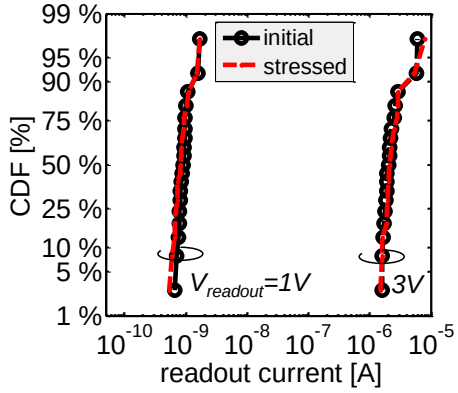


Figure 4.44: *Cell current distribution before (circles) and after (dashed lines) application of a thermal stress of 125°C for 3hours, at different biases. All currents are read at 125°C. Data collected on 40nm devices.*

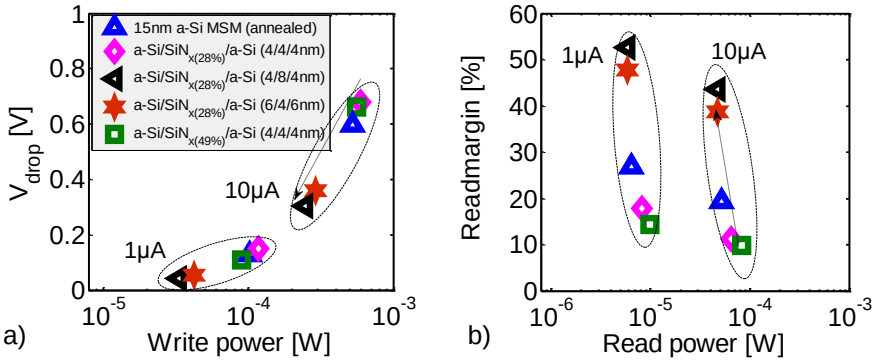


Figure 4.45: *(a) Simulated access voltage drop and write power for array size up to 1Mbit using 1S1R$_{(default)}$ cell, where using experimental I-V of MSM and TSI selector as reference. (b) Simulated read margin and read power. Different RSE switching current level, e.g. 10µA to 1µA are compared.*

4.5 1S1R array performance exploration

To confirm the feasibility of the MSM selector for cross-point arrays, circuit simulations have been performed. The I-V characteristics of the 1S1R cell are constructed by combining the default RSE model (section 3.2.2) and the experimental I-V sweeps of the proposed MSM and TSI selectors. The operation of the full 1S1R cell would require voltages around ±5V (not shown), which are considerably lower than voltages used for standalone NAND Flash memory in the range of ±20V. The full cell operating voltage range can be reduced by decreasing the operating voltage of a selector. However, this would diminish full cell non-linearity, especially for the write operation (section 3.2.3).

The array simulation is then performed using the framework as introduced in Chapter 2, assuming 1Mbit (1024x1024) array with an ½-bias scheme. The simulation results (Fig.4.45) are consistent with Fig.4.32, revealing that a highly non-linear selector improves both read and write performance. The TSI selectors with a-Si/SiN$_x$/a-Si thickness combination of 4/8/4nm and 6/4/6nm show the best NL½ of over 6000. This leads to the smallest access voltage drop (V$_{drop}$) due to the line resistance during the write operation (Fig.4.45.a), the largest read margin (Fig.4.45.b), as well as the lowest read/write power consumption (Fig.4.45). The figures-of-merit for array performance can be further improved, provided the RSE switching current reduced from 10µA to 1µA range, as expected.

4.6 Conclusion

In this chapter, we proposed a novel Metal/Silicon/Metal (MSM) selector using ultra-thin undoped amorphous silicon (a-Si) for resistive memory selector applications. By including annealing and barrier engineering, we show optimized MSM structures with superior performance with high drive current exceeding 1MA/cm^2 and half-bias non-linearity over 6000. Excellent reliability is demonstrated, with statistical ability to withstand bipolar cycling of over 10^5 at drive current condition. The trap generation in the a-Si layer is responsible for the selector degradation, affecting its non-linearity and current drive. Finally, the array sizing simulation results suggest that NL½ is a proper figure-of-merit for benchmarking the selector performance, selector with larger NL½ provides better array read and write performance. With the best selector structure, less than 0.4V voltage drop during the write operation and over 45% of read margin is expected for 1Mbit array. Array level performance is expected to improve further, by reducing the switching current of a resistive switching memory.

Chapter 5

Impact of device variability on the 1S1R array performance

5.1 Introduction

The intrinsic variability [59–61] inherent to the Resistive Switching Element (RSE) significantly affects the performance of the cross-point arrays. Large spread of LRS and HRS resistance levels affects the functionality of the cross-point arrays [20, 167]. Recently, circuit simulations results were reported [132,134,168], to evaluate the impact on array operation of the variability caused by the RSE only. The results indicate an even worse readout current distribution at array level compared to that at device level. For large arrays, the impact of variability is magnified due to leakage currents from the unselected devices, which leads to additional spread to the total readout current. However, a limitation of the previous results is that the selector element impact is excluded from the analysis and the extent to which the selector variability may affect the array operation is not known.

In this chapter, a variability-aware 1S1R array performance assessment methodology is proposed, which accounts for both selector and RSE variability, as well as for the data pattern randomness. We focus on the impact of variations during the read operation, since according to our previous simulation results, the read-out remains the more critical operation than write when the array size increases. By injecting selector variability using the experimental data from our reference MSM selector (detail in Chapter 4), our analysis points out that the selector element is an important array variability contributor, which mainly increases the dispersion of the LRS readout current, thus degrading the overall read performance. Therefore, an additional margin in selector NL½ and a

minimal 1R tail-to-tail resistance window (RW) are required to accommodate selector variability and to guarantee acceptable read performance.

This chapter is organized as follows: in section 5.2, we introduce the methodology for the variability-aware 1S1R performance assessment; in section 5.3, the 1S, 1R cell requirements are extracted considering variability contributions from both elements of the 1S1R cell. Finally, the main results are summarized in section 5.4.

5.2 Cell variability quantification for the 1S1R cell read performance analysis

5.2.1 Variability affected device model

Variability impact in circuit simulation is accounted for, by enabling parameter variation in an analytical component model [123]. These parameter variations allow a circuit simulator to predict the circuit response under various conditions, in order to optimize the final design. Within the scope of this work, we aim at identifying the main variability contributors in the array, considering different possible variability sources. Therefore, to quantify variability, we take the simplest approach: we use experimentally available data from our reference selector (annealed 15nm a-Si MSM selector, as discussed in Chapter 4) [127]. Moreover, we describe the RSE by allowing for variations in the R_{HRS} and R_{LRS}, in line with the typical variability from recent reports, while maintaining a generic 1R element definition.

a) The Metal-Silicon-Metal selector

We refer to TiN/amorphous-Si/TiN (MSM) selector devices [127] (Chapter 4), fabricated using a crossbar process. The I-V characteristics are measured from a reasonably large amount of cells of nominal size (40x40nm^2) to offer a $\pm 3\sigma$ description (Fig.5.1.a). The cell readout current, collected at a predefined voltage applied across the structure, fits the normal distribution. The normalized (dimensionless) standard deviation parameter, σ_r=σ/μ (σ: absolute standard deviation, μ: mean) is employed to quantify the device-to-device (d2d) variation (Fig.5.1.b). The normalized standard deviation shows typical values ranging between 0.2 and 0.4. For low bias, the relative standard deviation increases, since the readout current is close to the noise level.

The variation in the MSM selector current is attributed to different sources: i) device geometry variation. e.g. small variation in cell area after patterning, and/or thickness of the a-Si layer. ii) impact of the defects in the amorphous silicon layer. If the device area is small, and the defect-assisted current component is relevant as a transport mechanism,

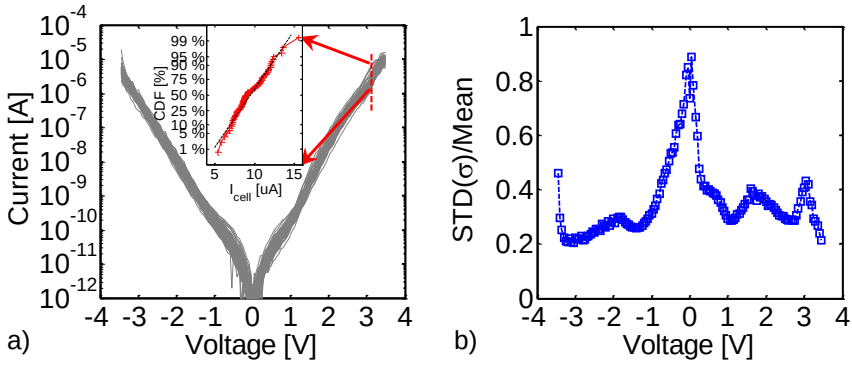


Figure 5.1: *(a) Experimental results of MSM cross-point selectors of 40x40nm^2 cell size. Inset: CDF plot of the readout current at specific voltage can be fitted with normal distribution. (b) Extracted 'σ_r=σ/μ' through the whole bias range.*

this depends on the particular spatial configuration of the defects in the cell. Note that, with a polycrystalline material, additional leakage non-uniformity could have been given by the presence of the grain boundaries [163]. This is however not applicable here, since the material has been shown to remain amorphous [127] by the end of the process. While the physical origin of the main variability source is of scientific interest, potentially providing feedback for device improvement options, for a device to circuit assessment, this is less important and we have chosen a single normalized standard deviation to describe the overall selector variability.

As an additional note, we observed no significant cycle-to-cycle (c2c) variation for the MSM selector, as the devices show excellent endurance, e.g. negligible degradation after 10^6 cycles at program and readout conditions, as shown in the previous Chapter 4.

b) The RSE (1R)

In filamentary switching [17, 59], the cycle-to-cycle (c2c) and device-to-device (d2d) variations are experimentally found to be numerically equivalent, therefore we do not differentiate between the two types of variation when modeling the RSE variability. For simplicity, both R_{LRS} and R_{HRS} are assumed ohmic. The median R_{LRS} is fixed at 50kΩ while the variability is injected into LRS with fixed normalized variation parameter: σ/log10(R_{LRS})=0.05 (Fig.5.2). We consider here two different scenarios for R_{HRS}. In the first case, median R_{HRS} is set at 500kΩ and a similar variation compared to that of the LRS is injected to the HRS, e.g. σ/log10(R_{HRS}) = 0.05. This corresponds to a median resistance on/off ratio of 10, and a tail-to-tail readwindow

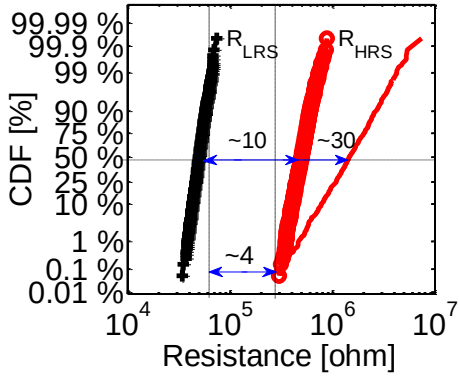


Figure 5.2: *Modeled characteristics of the RSE read-out resistance distributions, assuming two cases for the HRS distribution: similar spread as for the LRS (cross) and larger spread compared to LRS (circles/line). The HRS median value has been adjusted so as to result in the same tail-to-tail on/off window.*

(RW) of about 4. However, for many RSE reported in literature [17, 59, 142, 169, 170], a larger spread of R_{HRS} is observed. Therefore, in the second scenario, we fix the median R_{HRS} at 1.5MΩ, while assuming a larger variation, e.g. σ/log10(R_{HRS})=0.2. In this way, the two R_{HRS} distributions have similar tail-to-tail RW of about 4, while the median RW is larger for the latter (~30). To limit the complexity of the generated results, we assume the first case (median RW equals to 10) as default 1R characteristics, unless otherwise mentioned.

5.2.2 Array simulation settings

a) Array configuration

The schematics of the simulated array is shown in Fig.5.3. Full circuit simulation (i.e. lump factor equals to one, R_{wire}=10Ω/cell) is performed, in contrast to the simplified (e.g. lumped) circuit model (as used in Chapter 3). For simplicity, a positive voltage is assumed. Furthermore, we fixed the readout voltage at +3.3V. This choice is given by the typical resistance values considered for our selector and RSE, under the constraint that in the worst case, the corresponding voltage drop over the RSE at readout does not induce disturbs. A ½-bias scheme is applied in this analysis, as an optimal bias, with respect to the minimal read power consumption. We monitor the readout current of the selected cell corresponding to the longest signal path during the read operation.

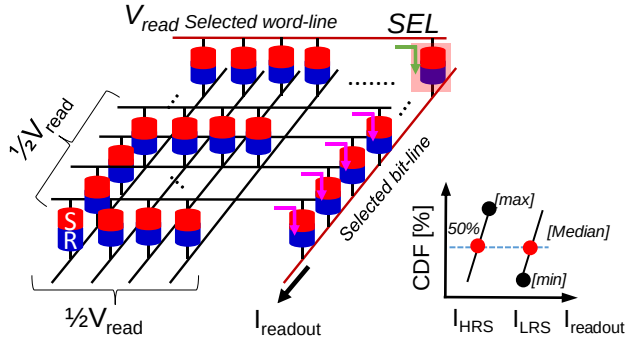


Figure 5.3: *Schematic of simulated array configuration assuming the ½-bias scheme. A line resistance R_{wire}=10Ω/cell is assumed (not shown).*

This corresponds to the worst case read situation. The bit line readout current consists of the actual cell readout current and the leakage from the unselected cells (including the cells connected to the selected bit line). In the worst case scenario, the number of cells that are connected to the reading path achieves its maximum, leading to the largest leakage current degrading the read signal. To quantify the read performance, a current-based definition of the read margin (RM) is defined, for both median and the worst case (tail-to-tail) situations:

$$RM_{median} = \frac{\Delta I_{readout}}{I_{ref}} = \frac{I_{LRS_{median}} - I_{HRS_{median}}}{I_{LRS_{median}}} \cdot 100[\%] \tag{5.1}$$

$$RM_{tail} = \frac{I_{LRS_{min}} - I_{HRS_{max}}}{I_{LRS_{min}}} \cdot 100[\%] \tag{5.2}$$

b) The Monte Carlo simulation loop

The variability-aware array performance assessment accounts for three distinct variability sources, namely the data pattern randomness, the selector and the RSE variation (Fig.5.4). Each of these variability sources can be injected into the circuit netlist separately or together with the others. A pseudo random number generator is used to generate instances of the array, with either one or several variability sources turned on. After each array instance generation, a SPICE simulation is carried out and the netlist is updated. Through this procedure, the read-out current can be calculated repeatedly, for a number of times, N, resulting in distributions that allow to assess the impact of variability for the considered situation (individual or combined).

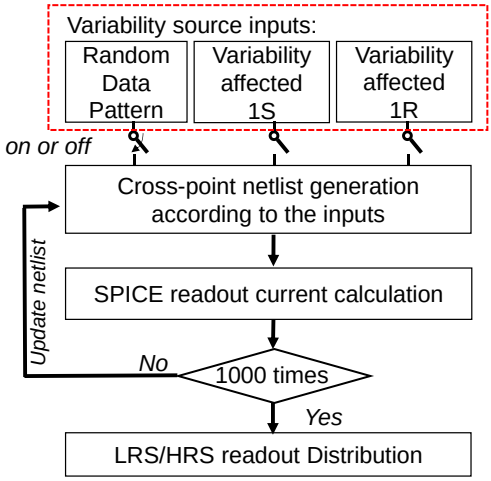


Figure 5.4: *Schematic of the Monte Carlo simulation loop for SPICE array level simulation taking into account 1S, 1R cell variability and data pattern randomness.*

5.2.3 Simulation results

5.2.3.1 Impact of the data pattern randomness

The 1R data pattern has big impact on read performance when considering 1R-only cross-point array without selector [132, 134, 168]. The spread of the readout current is amplified due to the variation of leakage current from the unselected cells. To evaluate the impact of the data pattern on the 1S1R array, RSE with different states (LRS or HRS) are randomly distributed across the array, with statistically 50% of cells in the LRS and 50% in the HRS. Other variability contributors are turned off, i.e. an ideal selector is assumed by taking the average MSM selector I-V, and R_{LRS}/R_{HRS} are fixed at their median values, i.e. 50kΩ/500kΩ.

A tight readout current distribution for reading both states is observed in the 1S1R array (Fig.5.5), in contrast to the 1R-only array [20, 167]. This is because the resistance (or the leakage current) of the unselected cells are dominated by the resistance of the selector element, irrespective of the states (LRS/HRS) of the RSE. In this way, the impact of data pattern randomness on the RM is effectively suppressed. Note that, when R_{HRS} becomes too large compared to the selector (i.e. the selector cannot select effectively, due to improper pairing with the RSE), the impact of data pattern randomness becomes significant (details in section 3.3.2).

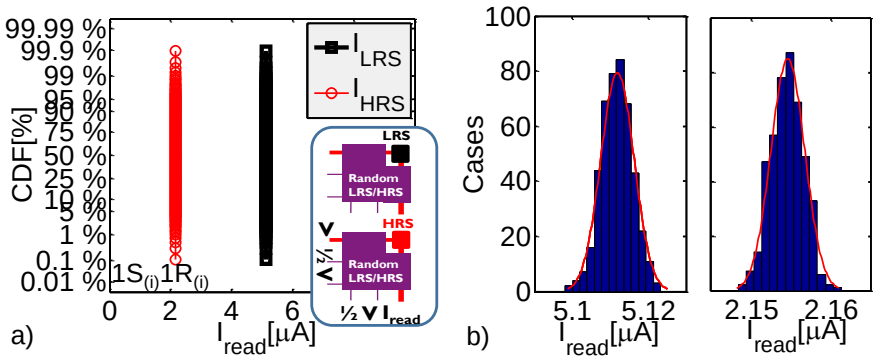


Figure 5.5: *(a) Read current CDF of ideal $1S_{(i)}1R_{(i)}$ cells, with variability-free 1S and 1R elements in an array with random data patterns show marginal readout current spread. (b) Column chart for I_{LRS} and I_{HRS} distribution. Data are on a 64x64bit array size.*

5.2.3.2 Impact of the selector variability

The ideal selector does improve the readout current distribution. However, a selector device displays variability, and that increases when the device area reduces, which may affect the read operation. To investigate this, variability-enabled 1S, ideal 1R and random data pattern generation are assumed as inputs for the simulation.

Selector variability affects the readout current in two ways. Firstly, it causes variation in the selected cell readout current (ΔI_{sel}), with respect to its nominal value, I_{sel}. Secondly, it leads to variation of the leakage current component of the unselected devices ($\Delta I_{leakage}$), relative to its reference value, $I_{leakage}$, so that the total readout current can be expressed as:

$$I_{readout} = I_{sel} + \Delta I_{sel} + I_{leakage} + \Delta I_{leakage} \tag{5.3}$$

Note that, the reference components in eq.(5.3) may, in principle, depend on the data pattern. To identify the dominant factor, we firstly freeze out the selector (i.e. disable variability) of the selected bit, while allowing selector variation to the rest of the array. In this way, ΔI_{sel} is removed and only the impact of the latter can be observed:

$$I_{readout} = I_{sel} + I_{leakage} + \Delta I_{leakage} \tag{5.4}$$

The CDF of the calculated readout current shows tight distribution when the selected cell is frozen, (Fig.5.6.a). This means the the selector variation caused by the unselected cells leads to limited $\Delta I_{leakage}$, and has almost no impact on the total readout current deviation.

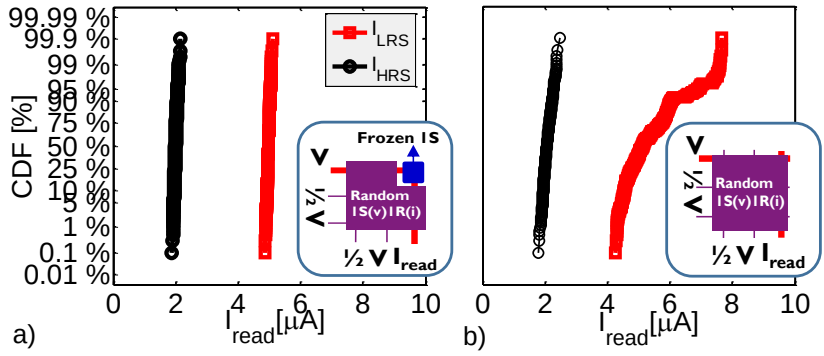


Figure 5.6: *(a) Readout current CDF. Including selector variability for all the cells except for the selected cell in the array. (b) selector variability for all the cells are enabled. Array size: 64x64bit.*

This also suggests that with an ideal 1R (e.g. tight R_{HRS}/R_{LRS} distribution during cycling) and highly reliable selector (i.e. no degradation after cycling), an excellent cycle-to-cycle readout behavior can be achieved for the 1S1R array.

In the next step, variability is further injected into all selectors in the array. As a consequence (Fig.5.6.b), the CDF of the readout current starts to spread. This indicates that selector variability of the selected cell is dominant. Due to the spread of the selector current, the d2d readout current distribution in the 1S1R array degrades.

Meanwhile, a large spread of the LRS readout current is observed in our results (Fig.5.6.b). This indicates that the LRS of the 1S1R cell is more sensitive to selector variability compared to the HRS. We then construct the 1S1R full cell characteristics by combining experimental selector I-Vs with ideal 1R characteristics (Fig.5.7.a). The normalized standard deviation, 'σ/μ' is extracted for the 1S1R device and compared with that of the 1S-only case (Fig.5.7.b). As expected, for both LRS and HRS states, the 1S1R variation is reduced in comparison with the 1S-only element after combining with an ideal RSE. The HRS shows much less variation compared to LRS since a larger fraction of the read-out voltage drops over the HRS element at readout voltage (e.g. +3.3V). Therefore, the variation of the selector parameters is more important for the LRS readout current. In this case, the relevant parameter is the selector resistance at readout voltage, which generates readout current variation.

The RM can be calculated for the worst case, median and the reference ideal case (i.e. using variability-free elements). In order to enable larger size array simulation for the ideal case, the simplified circuit netlist (discussed in Chapter 2) was employed. The difference between median and ideal cases is negligible. Due to selector variation, the

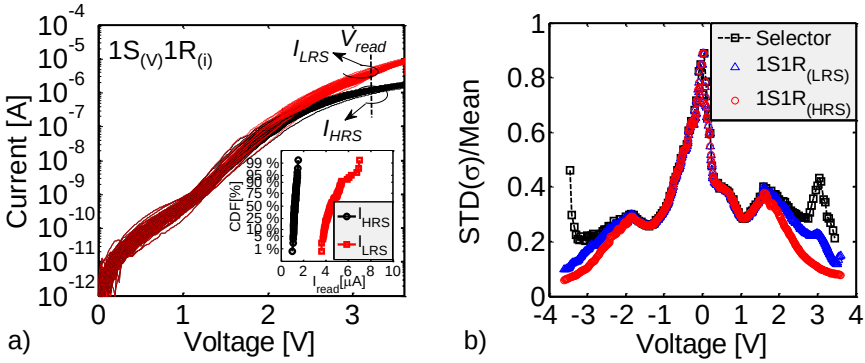


Figure 5.7: *(a) Constructed $1S_{(v)}1R_{(i)}$ cell IV characteristics for both LRS/HRS states, with experimental (variability-affected) selector IVs and ideal (variability-free) 1R characteristics. (b) Current variation at readout condition is suppressed when combing with ideal 1R device.*

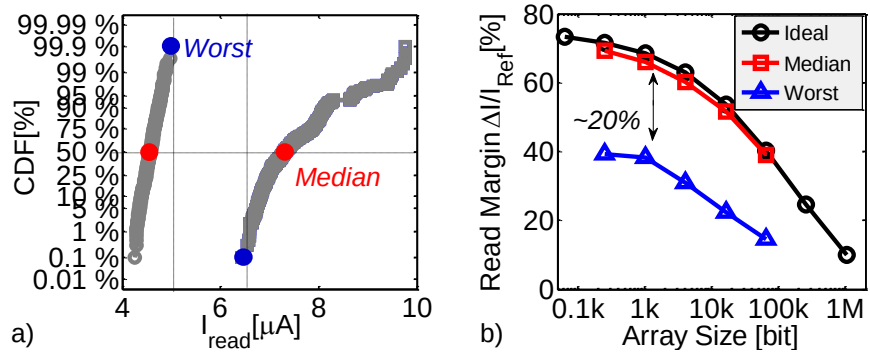


Figure 5.8: *(a) Readout current distribution for 64kbit array: 256x256. (b) Selector variability impact on the RM, for the worst-case, median and ideal case.*

readout current distribution spreads out (Fig.5.8.a), causing a worst case (i.e. tail-to-tail) RM decrease by around 20% compared to the ideal case and median (Fig.5.8.b). Because of the computation time limitations, in this case, 64kbit (i.e. 256x256) is the maximum array size considered for simulating the circuit when including cell variability.

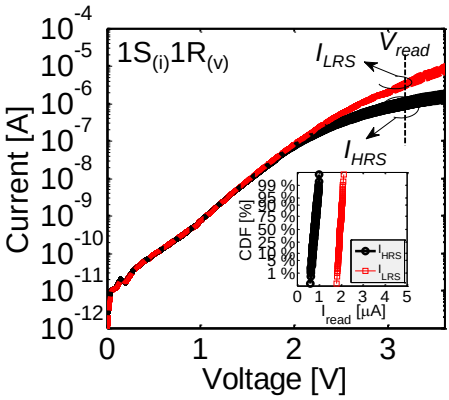


Figure 5.9: *Constructed $1S_{(i)}1R_{(v)}$ cell IV characteristics for both LRS/HRS states, with variability-affected RSE IVs and ideal (variability-free) 1S characteristics.*

5.2.3.3 Impact of the RSE variability

Conversely, 1R-only variability is enabled while assuming an ideal selector. The 1S1R full cell characteristics are constructed by combining the average selector I-V with the variability-affected 1R characteristics (e.g. R_{HRS}/R_{LRS}(median)=10, tail RW~4). It can be seen (Fig.5.9) that the RSE resistance variation affects both LRS and HRS current at readout voltage. However, its impact on the low-bias leakage current is limited, since the current is mostly determined by the ideal selector. Therefore, similar to the previous analysis, it is clear that the 1R variation will not influence the leakage of the unselected cells. When injecting RSE variation, the readout current variation is mainly impacted by the selected cell itself.

We compare the 1S1R readout current distribution, by combining selector with different 1R characteristics (Fig.5.2), i.e. R_{HRS}/R_{LRS}(median) equals to 10 and 30, respectively. Resistors either in LRS or HRS are randomly distributed in the array (data pattern randomness is turned on). The CDF of the calculated readout current indicates that by increasing the RW median of the 1R element from 10 to 30, the median readout current of the 1S1R only reduced by about 0.6μA (Fig.5.10). The 1S1R readout current tail is mainly affected by the 1R tail-to-tail RW. In our case, no difference is observed for the tail of the readout current in the HRS between the two scenarios, since we assumed the same tail-to-tail RW for the 1R element. As an illustration (median RW=10), due to the R_{LRS} and R_{HRS} variation, a total penalty of about 18% of the RM degradation is observed compared to the ideal case where all the variability sources are turned off (Fig.5.11).

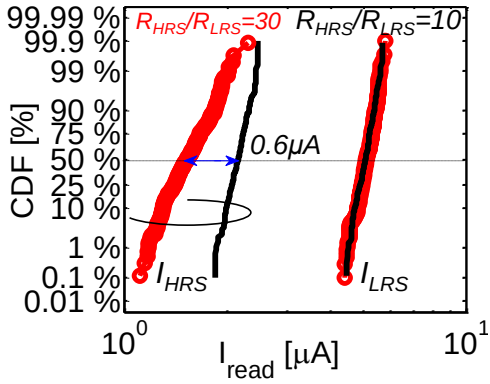


Figure 5.10: *CDF of the readout current, assuming two different HRS distributions of the RSE (1R element): R_{HRS}/R_{LRS}=30(circle), R_{HRS}/R_{LRS}=10(line), the tail-to-tail window remains the same. Array size: 64x64bit.*

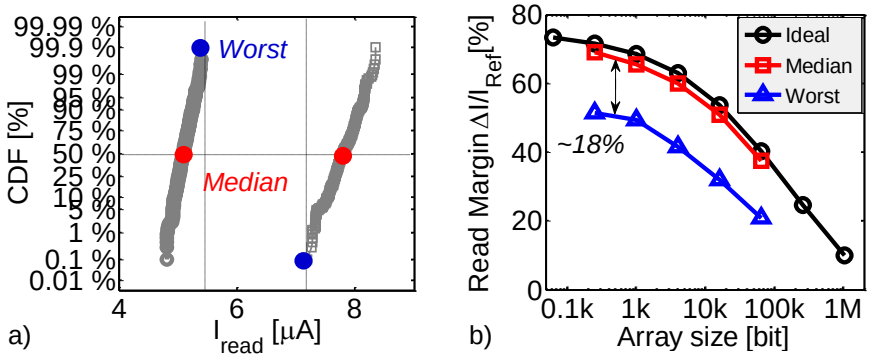


Figure 5.11: *(a) Readout current distribution for 64kbit array: 256x256. (b) RSE variability impact on the RM, for the worst-case, median and ideal case*

5.2.3.3 Impact of all variability sources

Finally, when all variability sources are activated, the net result is an even larger distribution spread of the readout current in both LRS/HRS states (Fig.5.12.a). The lower LRS readout current tail results in a total penalty on the RM of about 30%, for the worst case (Fig.5.12.b). In contrast to RM degradation, the upper tail of LRS readout

current increases the power consumption in the worst case. However, the impact is limited (Fig.5.13).

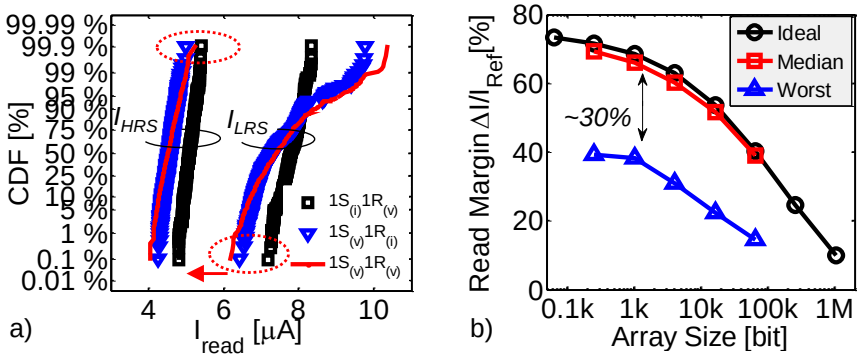


Figure 5.12: *(a) Readout current distribution for 64kbit array: 256x256. A larger spread is observed when all variability sources are turned on. (b) 1S, 1R variability impact on the RM, for the worst-case, median and ideal case.*

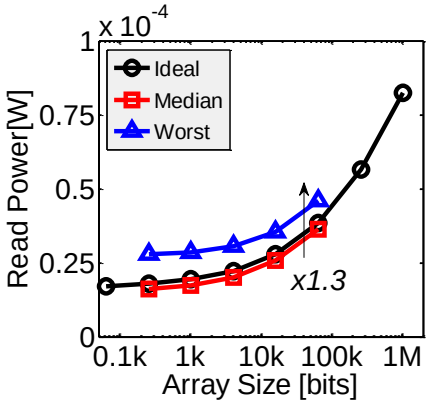


Figure 5.13: *Read power vs. array size when all variability sources are turned on for the worst-case, median and ideal case. Cell variation impacts on read power, although present, is lower compared to that on the RM.*

5.3 Extraction of the 1S1R requirements considering cell variability

So far, based on the experimental results of MSM selector and the assumed R_{HRS}/R_{LRS} distribution, we introduced the variation into the 1S and 1R elements, respectively, for simulating characteristics of the array size. By injecting individual and multiple sources of variability in the 1S1R array, we show that the data pattern randomness is not a concern in the 1S1R array as long as the selector dominates the leakage currents of the unselected cells. The 1R variation decreases the array RM. On top of that, we show that the selector is another important array variability contributor and it mainly affects the LRS readout current, which degrades the RM. Therefore, to accommodate cell variation and guarantee acceptable read performance, improved cell characteristics are required to enable a robust, variability-aware 1S1R array design.

In this part, we further derive the 1S1R cell requirements under the assumption that both elements are affected by variability, in contrast to our previous analysis (Chapter 3) where ideal 1S and 1R characteristics are assumed. Considering the fact that the 1S1R array targets high density memory applications, we expand the simulation capability for assessing 1Mbit array performance in a computationally efficient manner.

5.3.1 Simulation settings

5.3.1.1 Array configuration

The simplified cross-point circuit model (Chapter 2) is employed for this study. In our analysis, the lump factor m is fixed at 4. This means that groups of 4 elements for the word-line half selected and bit-line half-selected cells, and 4x4=16 elements for the non-selected (NS) cell are formed. As a result, 1Mbit array circuit is reduced to an equivalent ~256x256 (64kbit) array.

Variability is injected into the simplified netlist in the following way, elements in the same group are assumed in the same state (LRS/HRS) and the 1S1R cell behavior (variability-free), while the behavior of 1S and 1R element differs for each groups. In this way, cell variability is injected across the whole array. As simulation resolution decreases when lumping elements together, a small lumping factor, e.g. m=4, is chosen, so as to get a good trade-off between the computation time and the accuracy.

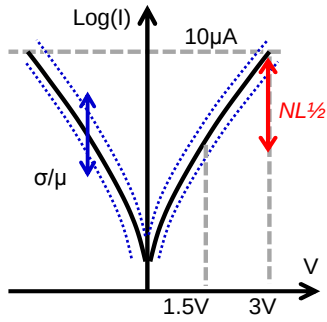


Figure 5.14: *Schematic of flexible selector template including device-to-device variation. Red solid line: average of selector characteristic.* σ_r=σ/μ *(*σ*: absolute standard deviation,* μ*: mean).*

5.3.1.2 Flexible selector template

Symmetrical selector characteristics are assumed, with the average I-V behavior modeled by a parametrized template using an exponential current-voltage equation. The selector drive current is fixed to 10μA at ±3V. A half-bias nonlinearity (NL½) is defined as the ratio between 10μA and current at |1.5V|.

A set of arbitrary numbers xi is generated following the normalized Gaussian distribution N~(1,σ_r), where σ_r is the normalized standard deviation, and the device-to-device variation is simply generated into the selector template, by multiplying average I(V) with x_i. With changing the variance σ_r, the spread of selector I-V characteristics can be tuned accordingly. Both NL½ and σ_r are free parameters, values of which can be varied independently. The schematic of the selector I-V characteristics is shown in Fig.5.14.

5.3.1.3 The RSE model

The 1R variation is modeled in a similar way as before, i.e. the median R_{LRS} and R_{HRS} are fixed at 50kΩ, 500kΩ, respectively. We assume constant variation for R_{LRS} with σ_{LRS}/$\log_{10}$(50k)=0.05, and consider σ_{HRS}/$\log_{10}$(500k) as a free parameter for R_{HRS}. By changing the R_{HRS} variance, different tail-to-tail RW can be obtained (Fig.5.15). In this study, three different scenarios are evaluated, namely for a tail-to-tail RW sets to 1.5, 3 and 5.

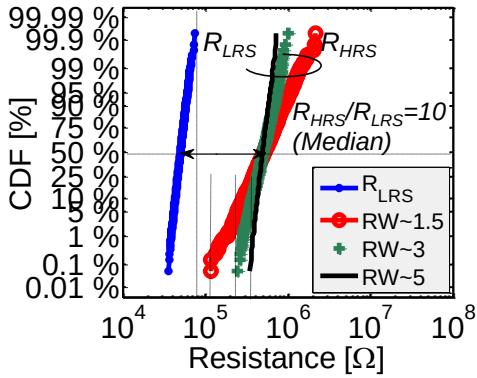


Figure 5.15: *Modeled 1R features: variations injected into both LRS and HRS states.*

5.3.2 Results and discussion

The simulation procedure as described in Fig.5.4 is employed. In this case, instead of injecting cell variation separately, all variability sources including selector, RSE and data pattern randomness are activated simultaneously for each simulation loop. A 10% difference of the readout current is defined as the minimal RM requirement, below which state separation is no longer reliable and can be easily affected by temperature variation, for example.

1S NL½ and 1R tail-to-tail RW are swept as free parameters while the selector variability parameter σ_r is fixed at 0.2. The calculated RM is plotted in Fig.5.16. If all the elements are ideal (close to median case), a selector with NL½=1000 is good enough to achieve the required RM. However, it is hard to achieve the same required RM due to the selector variability and closure of the tail-to-tail RW of the RSE (e.g. RW<5), even though the selector provides a large NL½ of about 10^4. This suggests a large tail-to-tail RW and an increase of NL½ are required to compensate selector variation.

With a fixed RW=5, the selector NL½ and variation parameter σ_r are considered as free parameters. Consequently, the calculated worst case RM is extracted to build second order response surface model [154](Fig.5.17). The data show that large selector NL½ is needed to accommodate selector variability for achieving the same RM. Most selectors reported in literature [81, 87, 89, 91, 94, 112, 127] show NL½ over 10^2, but hardly exceeding 10^4. Fig.5.17 (red dot) suggests a reasonable example for 1S1R cell parameter design target, where a selector variation σ_r=0.2, a minimal (i.e. tail-to-tail) RW equals to 5 and selector NL½ of about 8000 (close to 10^4) are required for a robust

1S1R design.

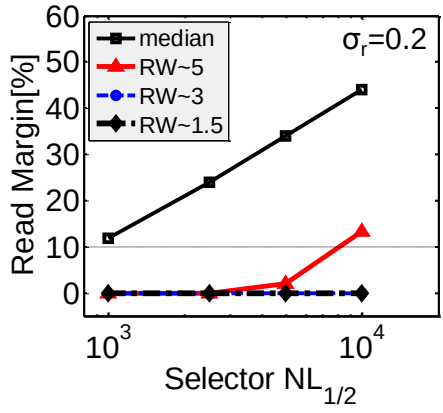


Figure 5.16: *Calculated RM as function of selector NL½ and 1R tail-to-tail RW, with fixed selector standard variation σ_r=0.2. Array size: 1Mbit.*

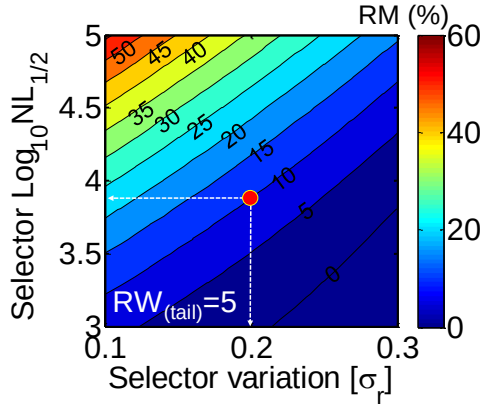


Figure 5.17: *RSM contour plot for calculated RM as function of selector NL½ and selector variation, with fixed 1R tail-to-tail RW=5.*

5.4 Conclusion

In this part, we presented a comprehensive simulation analysis that investigates the impact of the cell parameter variations on the overall 1S1R read performance. The variability-aware array performance assessment accounts for three independent variability sources: data pattern randomness, selector and RSE variation. By injecting these sources of variability in the 1S1R array, either separately or simultaneously, we show that the data pattern randomness is not an important factor for RM degradation as long as the selector limits the leakage currents of the unselected cells (i.e. the selector contribution to the total 1S1R cell resistance is dominant). The tail RW of 1R affects the worst case RM. On top of that, the selector is another important array variability contributor and mainly affects LRS readout current, causing extra RM degradation. To accommodate cell variation and guarantee acceptable read performance, improved cell characteristics are required to enable a robust, variability-aware 1S1R array design. We further assessed the 1S1R cell requirements for a 1Mbit array including cell variability. With a selector variation σ_r=0.2, a minimal RW of 5 and selector NL½ of about 8000 are required to obtain 10% of RM.

Chapter 6

3D RRAM

6.0.1 Introduction

Several 3D architectural concepts have been considered [47, 48, 68, 119, 171–174] to further reduce the bit-cost for resistive memory as post-NAND applications [7] and Storage Class Memory (SCM) [27, 28]. Stacking 3D cross-point arrays [68, 119, 171–174] does improve memory density. However, it requires critical process steps (e.g. lithography and etch) for each additional memory layer. This introduces extra process complexity and increases the fabrication cost [47]. Recently, vertical cross-point RRAM (VRRAM) [47, 48] similar to the BiCS (Bit Cost Scalable) approach used for 3D Flash [6, 175] were suggested. In this structure, a single critical lithography and etch step is used to define cells on different layers, which is more cost effective. Electrical behavior of single-layer 2D cross-point arrays has been analyzed in several publications [76, 113–115, 121, 122, 128–134, 176] and also in the previous chapters of this thesis. Most of the conclusions can be applied to stacked 3D array due to the similar structures. However, an analysis of VRRAM arrays [177] is still lacking. In this chapter, we extend our simulation framework (Chapter 2) to enable a quantitative analysis of VRRAM architectures.

This chapter is structured as follows: in section 6.2, we first review the different architectures for 3D RRAM, namely the stacked cross-point array and vertical array; in section 6.3, we focus on the proposed VRRAM and investigate the read and write operations in VRRAM arrays considering the worst-case data patterns. Different bias schemes are compared, and the optimal write bias scheme is determined for VRRAM; in section 6.4, a comparison is made between stacked 3D RRAM and VRRAM arrays. The final conclusions are drawn in section 6.5.

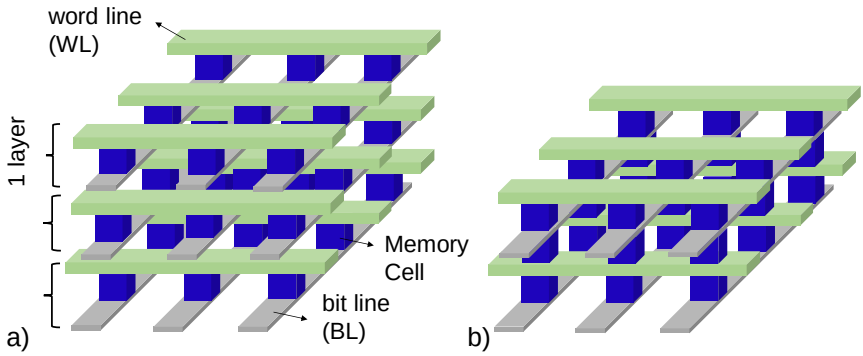


Figure 6.1: *(a) 3D stacking architecture with isolation in between two neighboring layers. (b) 3D stacking by sharing the WLs and BLs between two adjacent layers. Memory cell can be either a self-rectifying RSE or a 1S1R cell configuration.*

6.1 Stacked and vertical RRAM structure

6.1.1 Stacked cross-point array

3D stacking that packs up multiple memory layers is an efficient way to further increase the effective density of the 2D cross-point arrays. In a simplest approach (Fig.6.1.a), an isolation layer is inserted between adjacent memory layers so as to avoid signal interference (e.g. leakage currents, disturbs, etc) [171] between the selected plane and the unselected planes. However, each individual layer requires 'n x n' interconnects. When stacking multiple layers, this leads to a large area overhead for landing all the interconnects to the peripheral circuits on the substrate. To reduce the peripheral area for interconnections, stacked 3D arrays, which share the interconnections between adjacent memory layers, have been proposed (Fig.6.1.b). This architecture reduces the number of interconnect lines as compared to the isolated-layer stack (Fig.6.1.a) to achieve the same memory capacity. However, it minimizes the lateral area required for arranging the interconnects, being employed in several RRAM array prototypes [68, 119]. However, the stacked 3D cross-point architecture is not that cost-effective if the number of layers becomes large. Stacking multiple cross-point arrays requires layer-to-layer alignment, patterning of interconnects and vias [171]. Multiple litho and etching steps significantly increase the manufacturing costs. Cost estimation has been made [47] on the shared WL_s/BL_s structure (Fig.6.1.b) showing that the number of critical masks will reach its cost-wise affordable limit (i.e. 20) when 8 memory layers are stacked [47] (Fig.6.2.a). Moreover, a cross-point array needs tight design rules to minimize lateral area consumption, when the feature size is less than 40nm and, expensive double

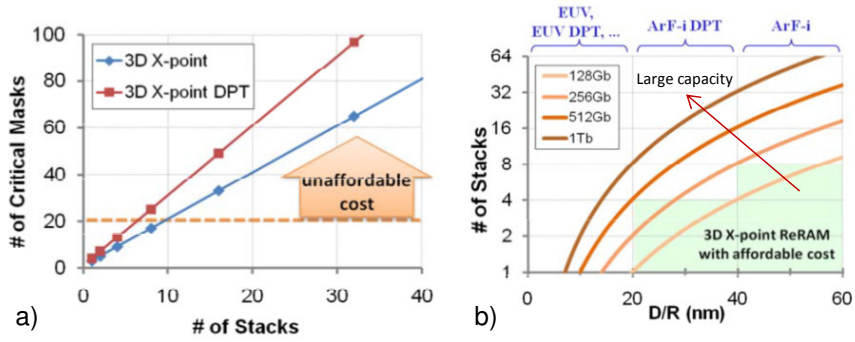


Figure 6.2: *(a) Required number of critical masks for 3D stacked RRAM vs. number of layers. DPT: Double Patterning Technology. (b) Number of layers as function of the design rule (D/R), for different memory capacities [47].*

patterning technology (DPT) is required. This would further complicates the process and as a consequence, the cost-wise number of layer reduces (Fig.6.2.a). Unless the cost of EUV goes down to be comparable with ArF immersion DPT, 3D stacking cross-point RRAM can hardly be extended beyond 512Gb (Fig.6.2.b), assuming 2-bit MLC [47]. Considering the current status, where the 3D Vertical NAND (VNAND) technology achieved 256Gb MLC in 32 layers [178], it appears unlikely that 3D stacked RRAM will become a replacement for future VNAND technology, targeting low-cost, mass data storage applications. To compete with continuous progress on 3D VNAND development, vertical cross-point RRAM (VRRAM) [47,48] using fabrication approach similar to that of VNAND [6, 175] is introduced.

6.1.2 Vertical cross-point array

In conventional 2D and stacked 3D cross-point structures, each cell can contain a RSE and a 2-terminal selector to suppress leakage currents from the non-addressed cells. However, such a separate selector is not appropriate in VRRAM since it would form a conductive electrode connecting the cells on the same (vertical) string, thus creating a short between neighboring cells (in adjacent planes). To isolate the cells, this inner electrode would have to be etched away, which is almost impossible (Fig.1.15). Furthermore, the presence of the extra conductive layer in the cell would limit the lateral scaling [47]. Therefore, VRRAM without a separate selector (e.g. using self-rectifying cell, SRC, as introduced Chapter 1) is required, both for high density and for proper operation [47]. Several reported SRCs [29, 47, 68, 179] have two functional layers

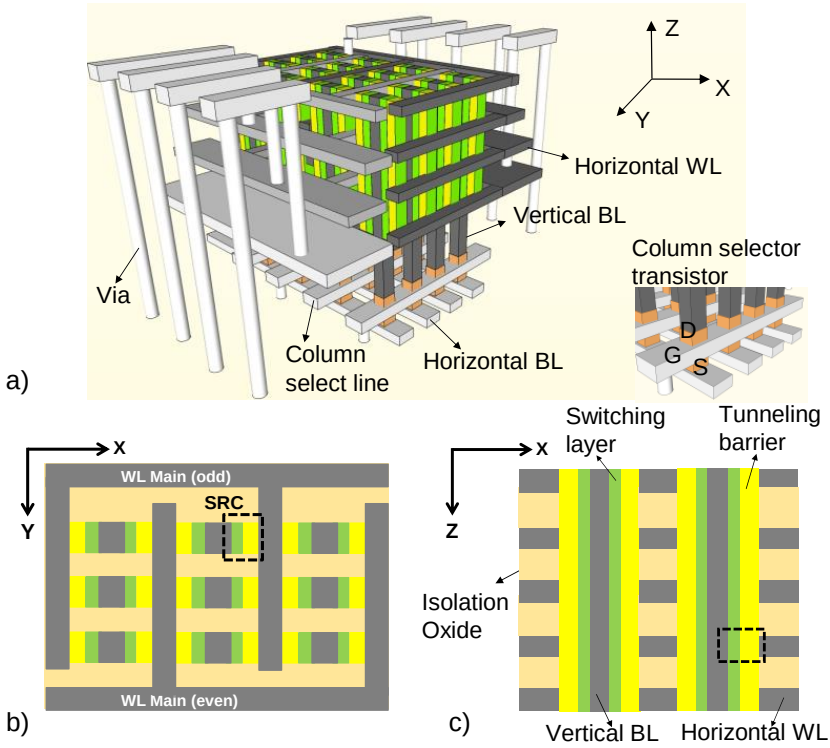


Figure 6.3: *Schematic of the proposed VRRAM (a) bird eye view (b) top view (c) side view.*

sandwiched by metal electrodes. One layer performs as a resistive switching medium and the other acts as a tunneling barrier providing non-linear characteristics.

In this work, we proposed VRRAM architecture as depicted in Fig.6.3. Each SRC is defined at the crossing of a vertical bit-line (VBL) and a horizontal word-line (HWL). In each plane, all WL_s are connected in two groups: even and odd WL_s. In contrast to stacked 3D RRAM, where each interconnect needs to be connected to the peripheral circuitry individually, this reduces the area overhead to connect WL_s to the WL drivers on the substrate. Each VBL pillar is connected to a column select transistor (e.g. a vertical transistor) at the bottom. During read or write operation, only one of the column select lines is enabled (e.g turn on the set of vertical transistors connected to this column select line), and all other BL pillars are floating (e.g. turn off the other transistors), reducing the total array leakage.

Other proposed VRRAM [47] (Fig.6.4) considers cylinder shape pillar structures where

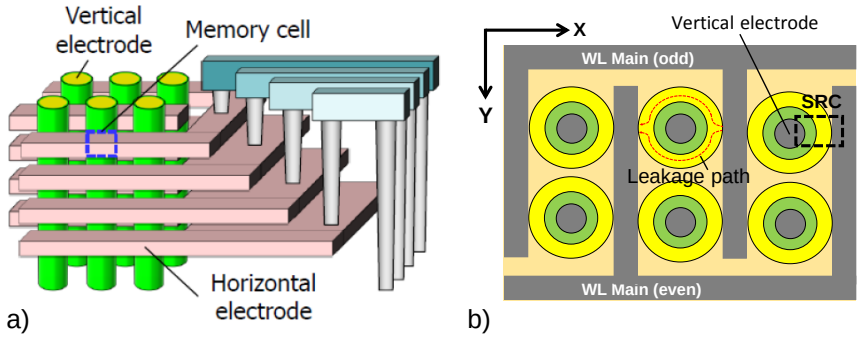


Figure 6.4: *(a) Bird-eye view of the cylinder-shape BL pillar VRRAM. (b) Top view. Reprinted from [47].*

each memory cell is defined at the tangent of the pillar and HWL. When a memory cell is selected, different voltages are applied to the odd/even WL forks on the selected plane. The voltage difference may introduce extra leakage currents between the neighboring cells (e.g. cells connected to the same vertical pillar) during memory operations. In contrast, this is not an issue for a trench-like VRRAM (Fig.6.3), since the adjacent memory cells on the same plane are fully isolated in the x-direction, thus the potential lateral leakage paths are cut off. Different from the previous structures, HWL_s for VRRAM [180] (Fig.6.5) can be formed without etching to a comb shape. Each SRC cell is defined at the cross-section between one VBL and WL plane (e.g. ring shape). Compared to the fork WL_s structure (e.g. one VBL defines 2 cells), the memory density is reduced. Moreover, due to the large surface area of un-etched metal plane, huge parasitic capacitance remains a potential concern for this architecture. This, could potentially affect the transient array behaviors.

VRRAM uses a similar process approach as compared to VNAND for achieving comparable fabrication costs. On top of that, VRRAM appears to have better scaling potential compared to VNAND for two reasons [49]: firstly, the lateral half-pitch of VRRAM is expected to be smaller than that of VNAND. The former is determined by the thickness of the SRC stack and pillar diameter, while the latter is determined by the minimal poly Si-vertical channel and charge trapping layer thickness. Secondly, due to the short channel effect, vertical cell-to-cell coupling and charge spreading issues, a minimum horizontal WL-to-WL distance for VNAND is required. For VRRAM, this distance is determined by the WL-to-WL parasitic leakages, which can be largely reduced when a good tunneling barrier is employed. Considering these two factors, VRRAM is forecasted to have about 2x in lateral scaling and x1.5 vertical scaling advantage over commercial VNAND technology [47], which is promising for further

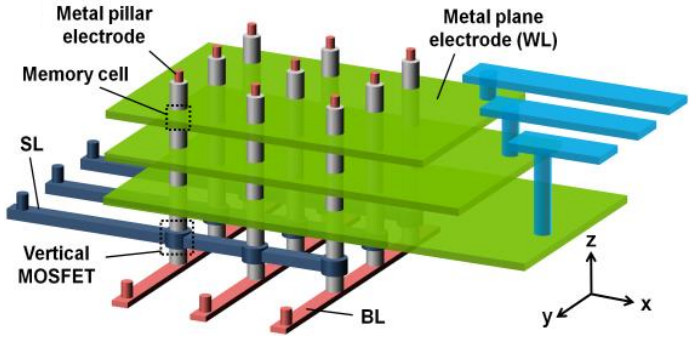


Figure 6.5: *Bird-eye view of the WL metal-plane 3D VRRAM structure. Reprinted from [180].*

reducing the bit-cost.

6.2 Analysis of vertical RRAM

In this part, a quantitative analysis on 3D RRAM is presented, focusing on the electrical behavior of VRRAM as depicted in Fig.6.3. A SPICE circuit model is developed for evaluating read and write performance of VRRAM, similar to the one implemented for 2D cross-point arrays (Chapters 2 and 3).

6.2.1 Simulation setup

The VRRAM array analyzed comprises k horizontal layers (x-y plane) of rectangular (nxn) bit arrays (Fig.6.3), the peripheral circuit is excluded in the SPICE model. Cells either in the LRS or HRS are assumed identical in the memory matrix, i.e. variability-free approach is employed. To ensure functionality, the worst case scenario is analyzed. We do consider the wire resistance inside the array (e.g. WL branches and vertical BL pillars with R_{wire}=10Ω/cell) while the parasitic capacitance is not considered. The selected cell located farthest from the main WL (i.e. at the end of WL branch) and horizontal BL (i.e. at the top plane) operates under the worst case operation condition (i.e. Fig.6.6.a, cell #1). To improve the simulation efficiency while maintaining Spice-level accuracy, the other components (e.g. cell and line resistance) can be partially lumped together according to their bias conditions, labeled as #2, #3, etc (similar approach to that introduced in Chapter 2). Finally, we assume ideal column select

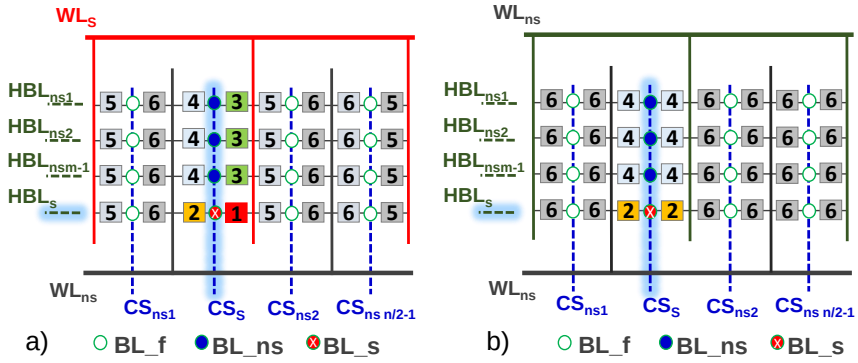


Figure 6.6: *Top view of VRRAM (a) the selected plane (top plane) (b) unselected plane (k-1). Cells with same number have similar bias condition. #1: selected cell (worst case cell) WL selected, BL selected; #2: WL unselected, BL selected; #3: WL selected, BL unselected; #4: WL unselected, BL selected; #5: WL selected, BL floating; #6: WL unselected, BL floating. Hollow dots (BL_f): floating BL pillar; solid dots (BL_ns): BL pillar connected to non-selected HBL; Cross (BL_s): selected BL pillar. HBL: horizontal bit line. CS: column select.*

Table 6.1: Applied voltages for the write and read operations using the ½ and ⅓-bias

Parameter	**½-bias scheme**		**⅓-bias scheme**	
	Write	**Read**	**Write**	**Read**
V_{WLs}	V_{dd}	V_{read}	V_{dd}	V_{read}
V_{WLns}	$\frac{1}{2}V_{dd}$	$\frac{1}{2}V_{read}$	$\frac{1}{3}V_{dd}$	$\frac{1}{3}V_{read}$
V_{HBLs}	0	$V_{sense(10mV)}$	0	$V_{sense(10mV)}$
V_{HBLns}	$\frac{1}{2}V_{dd}$	$\frac{1}{2}V_{read}$	$\frac{2}{3}V_{dd}$	$\frac{2}{3}V_{dd}$
CS_s	on	on	on	on
CS_{ns}	off	off	off	off
V_{BL_f}	floating	floating	floating	floating
V_{BL_ns}	$\frac{1}{2}V_{dd}$	$\frac{1}{2}V_{read}$	$\frac{2}{3}V_{dd}$	$\frac{2}{3}V_{dd}$
V_{BL_s}	0	$V_{sense(10mV)}$	0	$V_{sense(10mV)}$

transistor. Voltage applied on the HBL_s can be transferred to vertical BL_s as long as the column select (CS) line turns on. The voltage distribution during the write and read operations under different bias schemes are compared, where the definition of ½ and ⅓-bias for VRRAM is listed in TABLE.6.1.

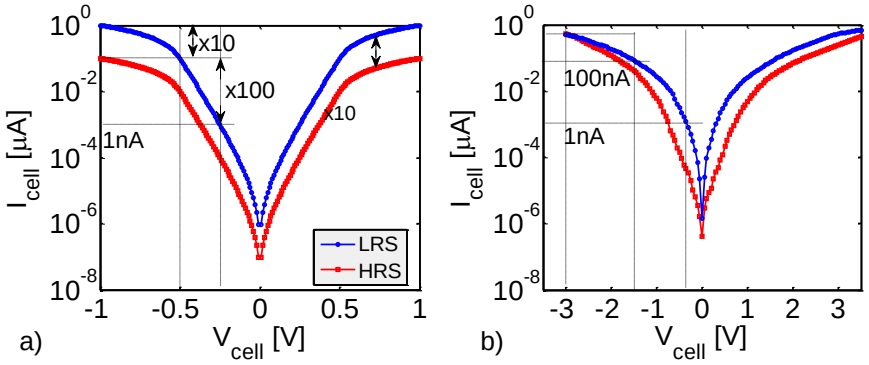


Figure 6.7: *(a) SRC device template. (b) behavior of an actual cell [68] for comparison.*

6.3.1.1 The SRC template

To focus our studies on the VRRAM architecture, the bipolar switching SRC is described using a parameterized template with fixed parameters (Fig.6.7.a). The behavior of cell template meets the features of an ideal non-linear RRAM cell, e.g. low switching voltage and current, self-rectifying behavior and large on/off resistance ratio. We fix the program voltage at $\pm$1.0V, the switching current is set at 1μA. A disturb voltage ($V_{disturb}$) sets to |0.5V|. The NL½ at write and read operation equals to 10 and 100, respectively. Note that we assume the read voltage (V_{read}) is the same as $V_{disturb}$, this ensures the minimal readout current being larger than 100nA. The on/off resistance ratio is set as 10 through whole I-V range. Compared to an actual SRC [68] in literature, this template has similar switching current and non-linear characteristics, but with a much lower switching voltage.

6.3.1.2 The worst case scenario

Single-bit operation is assumed, i.e. only one cell of a full local array is programmed or read at a time. The worst case data patterns are given in TABLE.6.2. For write, the worst case data pattern is when all cells are in LRS. This results in the highest leakage current, power consumption, and the largest voltage drop over the interconnects. We do not differentiate the set/reset operations, as the cell template has symmetrical I-V behavior. For read, the current on the selected BL pillar is the sum of the read current of the selected cell (#1) and the current of the BL half selected cells (#2). With read margin (RM), we used the same definition (Chapter 2). For the required RM, we assume 25% as the minimal requirement.

Table 6.2: Applied voltages for the write and read operations using the ½ and ⅓-bias

Write	Read '0'	Read '1'
All LRS	Selected cell (#1):HRS Cell (#2):LRS Cell (#3-#6):LRS	Selected cell (#1):LRS Cell (#2):HRS Cell (#3-#6):LRS

6.2.2 Results and discussion

6.3.2.1 Read operation

Fig.6.8.(a) indicates a significant reduction of RM with increasing the number of layers. The main cause of this the degradation is that more cells are connected to the selected VBL pillar, which gives more leakage currents. The extra leakage makes it more difficult to discriminate the selected cell (#1) state.

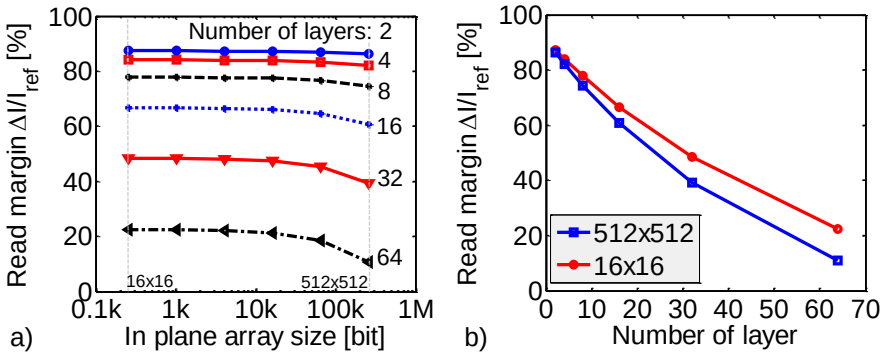


Figure 6.8: *(a) Simulated read margin as a function of array size using ½-bias scheme (a) The read margin decreases with increasing number of layers (b) The number of cells in the horizontal plane (x-y) has less influence on the read margin. In plane array size from 16x16 (0.25k) to 512 x512 (256k) were considered.*

The RM is less affected by the in plane (x-y) array size (Fig.6.8.b), because increasing the array size (x-y) does not add extra leakage paths on the selected BL pillar directly (1^{st} order effect on RM). However, with the increase of wire resistance for larger arrays, the actual voltage seen by the selected cell becomes smaller. Fig.6.9 indicates that the voltage across the selected cell is smaller when reading LRS than reading HRS when considering the worst case data patterns. This leads to a decrease (2^{nd} order effect)

of the RM. However, in our simulation, the impact is very limited due to the large R_{HRS}/R_{wire}, R_{LRS}/R_{wire} ratio and a low current operation.

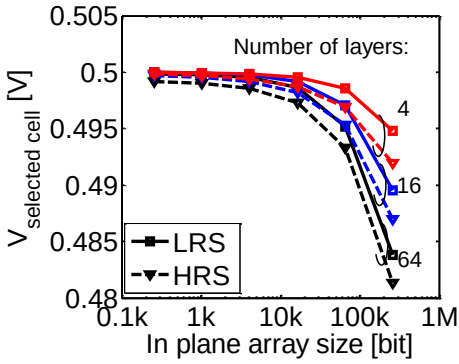


Figure 6.9: *Actual voltage seen by the selected cell becomes smaller for larger in plane (x-y) array size, V_{read}=0.5V.*

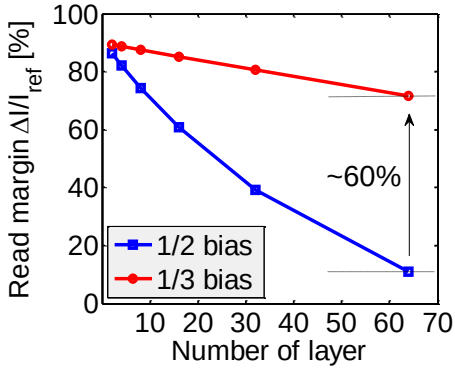


Figure 6.10: *Using ⅓-bias scheme leads to larger RM for the same matrix size, as it decreases the voltage across the bit-line half selected cells (#2) compared with ½-bias. In plane array size: 512x512.*

A trade-off between RM and read power consumption is observed by comparing different bias schemes. The simulation results show that the RM is much larger when using the ⅓-bias scheme (Fig.6.10). This is because in a ⅓-bias scheme, voltage

on the unselected WL_s (WLNS: ⅓V_{read}) is smaller than ½V_{read} and the BL half selected cells (#2) see smaller voltage, therefore providing less leakage currents. The power consumption becomes larger when using ⅓-bias instead of ½-bias (Fig.6.11). Moreover, Fig.6.11 suggests that the power is strongly affected by the in plane array size (x-y) while it is much less sensitive to variations of the number of stacking layers. This implies that the selected plane is more important than the unselected ones for determining total power consumption (i.e. most of the power consumption comes from the selected layer).

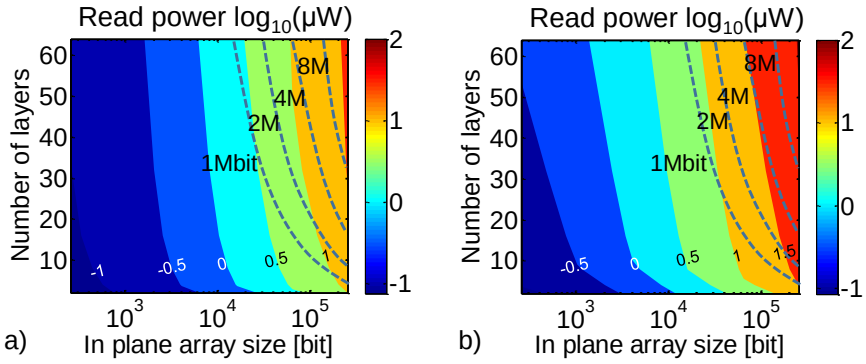


Figure 6.11: *Read power consumption (scales on the colour bar) in (a) ½-bias and (b) ⅓-bias. Dash line indicates memory capacity from 1Mbit to 8Mbit.*

To explain this, two types of selected WL branches on the selected plane, namely the WL B1 and B2 are further analyzed, (Fig.6.12.a). For B1, half of the cells connected to it can be biased and half are floating. All cells connected to WL B2 are floating. The leakage on B2 strongly depends on the voltage of the floating VBL pillars, which is affected by voltage difference (V_{WLS}-V_{WLNS}). The larger the difference, the larger (V_{WLS}-$V_{floating}$) and (V_{WLNS}-$V_{floating}$), and consequently, cells #5 and #6 provide more leakage. (V_{WLS}-V_{WLNS}) equals to ⅔V_{read} for ⅓-bias, which is larger than ½V_{read} for ½-bias scheme, thus the leakage currents on B2 are larger. Leakage on B1 depends on both the biased BL pillars and floating ones. For VRRAM, there is only one WL B1 but many WL $B2_s$. Therefore, using an ⅓-bias scheme leads to larger total leakage and more power consumption. On the other hand, WLs in each unselected plane have the same bias, e.g. (V_{WLNS}-V_{WLNS})~0V. Consequently, the power consumed by the unselected planes is limited, which explains the results in Fig.6.11, i.e. limited impact on the power by adding more memory layers.

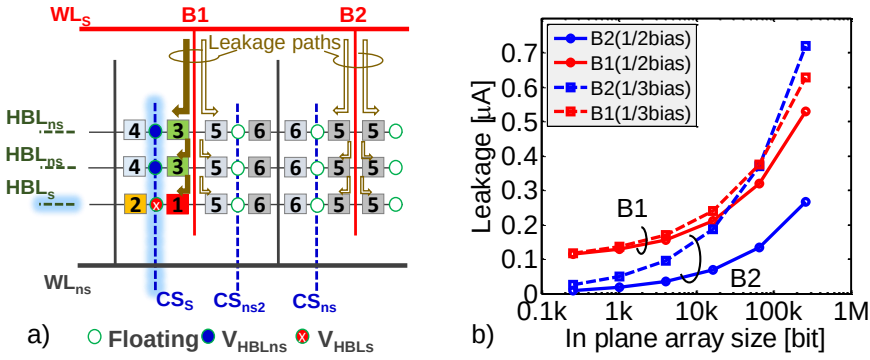


Figure 6.12: *(a) Current flowing on the selected plane of VRRAM, two types of selected WL branches are defined: B1 and B2. (b) Observing the leakage on B1 and B2 reveals that reducing the voltage difference between selected WL and unselected WL branch raises the voltage on the floating BL pillars, less leakage on B2 is obtained. Leakage current on B1 depends on the voltage of both floating points and the biased BL pillars. ½-bias is better than ⅓-bias for reducing the leakage currents.*

6.3.2.2 Write operation

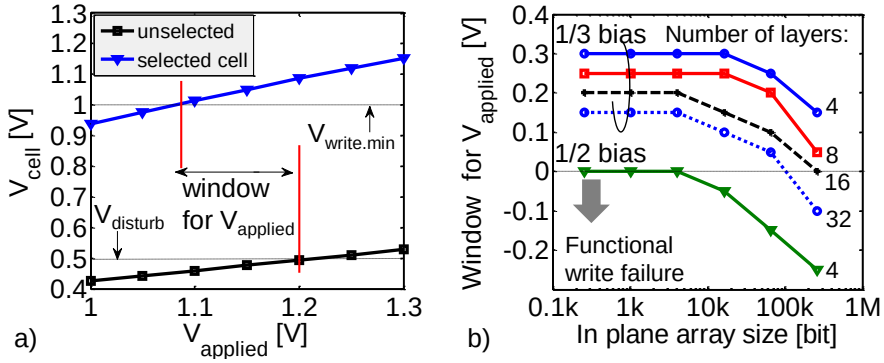


Figure 6.13: *(a)Window for applied program voltage in 256x256x16 VRRAM array under ⅓-bias (b) Window for $V_{applied}$ as function of array size. Increasing in plane array size (n x n) and number of layers both decrease the voltage window for write operation.*

The line resistance effect is more significant for the write operation since higher voltage and currents are involved. An inhomogeneous voltage distribution may lead to write disturb or fail. The window for the applied program voltage is defined as the maximal voltage that can be applied over the selected cell in excess of the voltage required to write it. This maximal voltage is limited by the fact that none of the other cells are allowed to be disturbed (e.g. 0.5V). A positive margin (i.e. 0.2V) is found for a 256x256x16 VRRAM array using ⅓-bias scheme as shown in Fig.6.13.(a). Fig.6.13.(b) plots the window for the write operation as function of array size. A much smaller margin is obtained using ½-bias scheme, because in our simulation, cell disturb voltage is |±0.5V|.

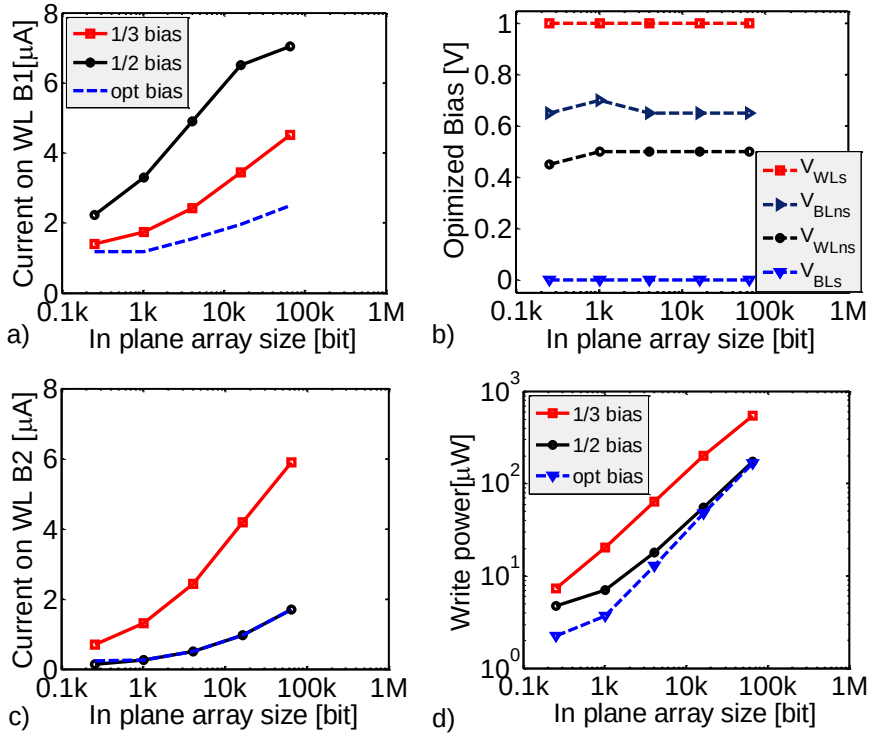


Figure 6.14: *(a) Leakage current on the selected WL branch B1 (b) bias condition for optimized bias scheme (ΔV=50mV) (b) Leakage current on the selected WL branch B2. (d) Total write power consumption under various bias scheme. Number of layers is fixed to 16.*

Another important concern for write is the total power consumption and the maximal

current allowed on interconnects (e.g. due to electro-migration limitation). To study this, an optimized bias scheme is compared with standard ones (e.g ½ and ⅓-bias). We set V_{BLS}=0V, optimize V_{WLS},V_{WLNS} and V_{BLNS} to minimize power consumption while ensuring the selected cell sees V_{write}. The maximal current on WL branch (B1 and B2) is smaller than 10μA and no disturbance occurs on the unselected cells. Fig.6.14 shows the simulation results for VRRAM with fixed number of layers equals 16, for various in plane array size.

Optimized bias schemes combine the advantage of both ⅓ and ½-bias scheme in a balance way, where it keeps (V_{WLS}-V_{WLNS}) low, e.g. ½V_{WLS} (Fig.6.14.b) to suppress the leakage current on the selected WL branch B2 (Fig.6.14.c), which reduces the total leakage and power consumption. Indeed, the write power for VRRAM is mostly consumed by cells #5 and #6, a large number of these cells are biased between (V_{WLS}-V_{WLNS}), Fig.6.15.(a). Optimal bias also lowers (V_{WLS}-V_{HBLNS}), e.g. close to an ⅓V_{WLS} (Fig.6.14.b), which reduces the leakage current on B1 (Fig.6.14.a), selected cell sees less voltage drop, in this way improving the window for applying the write voltage avoid disturbance. For large in-plane array size (e.g. many WL B2), the leakage current on WL branch B2 (i.e. through cell #5, #6) becomes the dominant factor that determines the total power consumption. As a result, the power consumption under optimal bias is similar to that of ½-bias (Fig.6.14.d). For small array size (e.g. lower number of B2), optimal bias consumes less power because the leakage on the WL branch B1 is small (i.e. less currents through cells #3). Optimized bias does not depend on array size, because V_{WLNS}= ½V_{WLS} is the maximum voltage can be chosen for unselected WL_s to avoid cell disturbance by #2. And V_{BLNS} = ⅔V_{WLS} is a balance bias value considering both the voltage drop on B1 and power consumption caused by cell #3 and #4.

6.3 Comparison between the stacked and vertical 3D RRAM

We consider the stacked 3D structure in which each memory layer is isolated (e.g. without sharing WL_s and BL_s). There is no interference between neighboring layers during memory operation. Therefore, stacked 3D can be analyzed in a similar way to that of a conventional 2D array (i.e. we can use to same analysis framework as we did in Chapter 2).

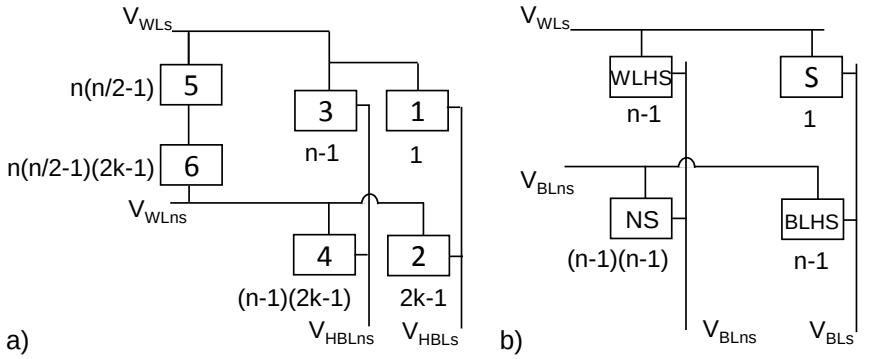


Figure 6.15: *Simplified schematics (excluding line resistance) of (a) VRRAM. n: number of cells along WL branch and WL. In plane array size: n x n; number of layers: k. (b) 2D cross-point array. n:number of cells along WL and BL. S:selected cell. WLHS: word line half-selected cells. BLHS: bit line half-selected cells. NS: non-selected cells.*

6.3.1 The read operation

The most important factor degrading the RM is the leakage current on the selected BL, this conclusion holds for both 2D array and VRRAM. A comparison between stacked 3D and VRRAM is shown in Fig.6.16, using the same input SRC template and assuming a fixed ½-bias scheme. The RM of stacked 3D and VRRAM show opposite trends. To achieve memory array of the same bit capacity, e.g. 1Mbit, in a stacked 3D solution, it is preferred to use a small in plane size but more stacked layers. Larger in-plane array size (i.e. large n) significantly degrades the RM due to the increase of cells (n-1) connected on the critical reading path (BL_s), Fig.6.15.(b). For VRRAM, however, the RM is more sensitive to the number of layers (k), as the number of cells on the critical path (HBLS) becomes (2k-1), Fig.6.15.(a). For this reason, large in-plane array size is preferred. Considering the cost for stacking 2D layers for stackable 3D structure, to further improve memory capacity, in plane array size has to be increased. This adds extra leakage paths to the selected BL, therefore, large cell non-linearity is required to achieve enough RM. However, increasing in plane array size for VRRAM causes limited RM degradation (Fig.6.8.b), cell non-linearity requirements can be relaxed for VRRAM compared to stacked 3D RRAM.

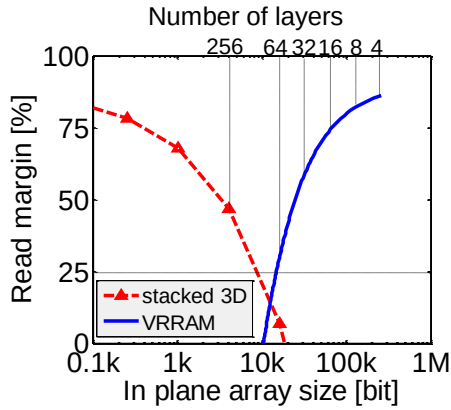


Figure 6.16: *To achieve the same memory capacity: n x n x k = 1Mbit. VRRAM has more advantage on read margin compared to stacked 3D structure for less layers and larger in plane array size structure.*

6.3.2 The write operation

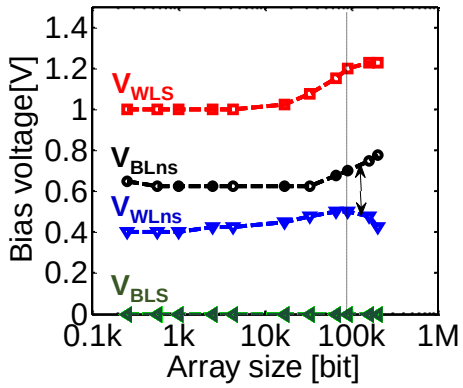


Figure 6.17: *Optimized bias for 2D cross-point array. Constraints: V_{write} on the selected cell, maximal leakage $\leq$10μA on selected WL and no disturbance occurs on unselected cells (ΔV=25mV). Only the voltage differences matter, it is possible to subtract e.g. 0.5V from all bias voltages.*

Optimized bias is determined to minimize the power consumption. Fig.6.17 plots the optimized bias conditions for conventional 2D. V_{WLS} increases with in plane array size due to the voltage drop on the selected WL and BL, thus more voltage needs to be applied to guarantee enough access voltage on the selected cell. V_{BLNS} increases as well, with respect to V_{WLS}, so as to keep the WL leakage under the pre-defined constraint (i.e. below 10μA) and avoid disturb occur. While V_{WLNS} almost remains with reference to V_{BLS} due to similar reasons. This would finally increases (V_{BLNS} -V_{WLNS}). In stacked cross-point array, $(n-1)^2$ non-selected (NS) cells are biased in this voltage region (Fig.6.15.b). This causes a significant power increase if the in plane array size becomes larger (Fig.6.18).

VRRAM, on the other hand, is more promising for large in-plane array size. Most of the unselected cells (e.g. cell #5 and #6, Fig.6.15.a) are biased between (V_{WLS}-V_{WLNS}) due to the floating BL pillars (Fig.6.15.a). Reducing (V_{WLS} –V_{WLNS}) not only reduces the power consumption, but also decreases the leakage current on the selected WL, i.e. VRRAM bypasses the bias trade-offs for balancing the voltage drop on the selected WL and power consumption. For small array size, VRRAM consumes more power compared to conventional cross-point arrays, because we cannot decrease (V_{WLS} –V_{WLNS}) further due to disturbance constraint for cell #2, e.g. (V_{WLNS}-V_{BLS}) below 0.5V. However, in conventional 2D, we can reduce voltage on the NS cells by accommodating more voltage on the rest of the cells, e.g. in Fig.6.17, optimized bias voltage difference $|V_{WLNS}$-$V_{BLNS}|$ below 0.3V for small array size (<100k bits).

Another issue associated with the write operation is the interconnect failure due to electo-migration (EM) when passing high current over the wires. For instance, 10μA current through 10x10nm^2 cross-section wire corresponds to 10MA/cm^2 current density, which exceeds the maximum limitation ~3.26MA/cm^2 [50] due to the EM failure (e.g. this constraint is specified for the high frequency logic circuits, while it can be relaxed for the memory applications [50]). For achieving target memory capacity, from the cost point of view (section 6.1.1), it is desired that stacked cross-point array has a limited number of memory layers but a large in-plane array size. This implies that the cross-point architecture needs tight design rule (e.g. to minimize the width and the space between interconnects) to achieve high-density memory block. As a consequence, cross-point array circuit is potentially subject to interconnects failure by EM. On the contrary, the lateral interconnect dimension can be relaxed for the VRRAM (e.g. bit-cost scaling is driven by stacking additional memory layers instead of pursuing aggressive lateral scaling), which is good for improving the circuit reliability.

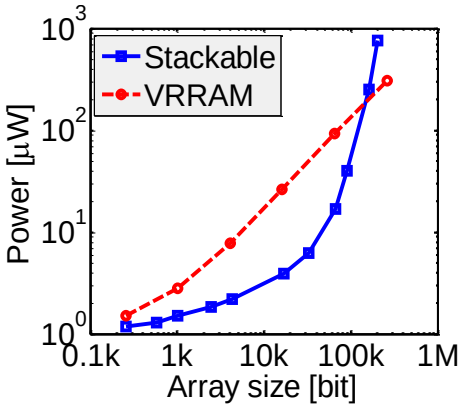


Figure 6.18: *Power consumption for conventional 2D and VRRAM under optimized bias condition. VRRAM consumes less power for larger array size.*

6.4 Conclusion

A quantitative analysis of VRRAM for both read and write operation is presented. The read margin is more sensitive to the number of layers compared to the in plane array size in the matrix. Reducing the voltage applied on unselected WL improves the read margin, however, it will increase the leakage current on selected WL and the total power. Write performance is more sensitive to bias conditions. Optimized bias conditions can be found for both improving the write margin and reducing the power consumption. Compared to stacked 3D architecture, assuming SRC with moderate non-linearity, VRRAM seems more promising for both read and write operations.

Chapter 7

Summary and outlook

This final chapter briefly reviews the main objective of the Ph.D. study (Section 7.1), summarizes the Ph.D. work and the main contributions and conclusions of this Ph.D. to the RRAM scientific community (Section 7.2); and finally gives an outlook of the future RRAM developments and suggests future work (Section 7.3).

7.1 Main Objective of the Ph.D.

The implementation of resistive memory into high-density memory array strongly depends on the availability of non-linear selector devices, to cut off the sneak currents during the memory operation. This Ph.D. study focuses on the electrical analysis on bit-cell level for the one-selector one-resistor (1S1R) cross-point resistive memory arrays, and by that aims at addressing the following two questions:

- What are the selector requirements for achieving an acceptable 1S1R array performance?
- How to make a selector device that fulfills these requirements?

To answer the above mentioned questions, both array-level simulation analysis and device-level experimental work were carried out.

The main objective of the simulation study is to understand the impact of selector characteristics on the overall cross-point array performance. Using a SPICE-based top-down approach, the requirements for selector are derived from a circuit perspective. The

simulation allows quantitative assessment of various selector concepts. Furthermore, it provides engineering guidelines for selector device development.

In addition, different selector concepts are evaluated experimentally, with the purpose of demonstrating a selector device that meets the target performance requirements, while fabricating in a CMOS-friendly process. Ultimately, amorphous silicon based Metal-Silicon-Metal (MSM) devices showing the best performance are chosen for an in-depth study to understand their performance, reliability and tradeoffs. To confirm the feasibility of MSM selector for cross-point arrays, circuit simulations were performed, further taking into account the selector variability.

7.2 Summary of this Ph.D. work

7.2.1 Major contributions of this Ph.D.

With the goal of exploring a proper selector device for 1S1R cross-point resistive memories, circuit-device interaction simulations, selector concept demonstration and device optimization were carried out. The major achievements and results of this Ph.D work are summarized as follows:

Chapter 2: We developed a cross-point array model and analysis methodology to be used for cross-point array simulations. The simulation framework includes an effective SPICE circuit model, which provides an efficient and accurate way to quantitatively analyze the relationship between the cell characteristics and memory array performance. The simulation platform enables array sizing simulations, as well as selector requirements derivation, which stands at the basis of the research work reported in this Ph.D. thesis.

Publications contributing to this chapter:

1. **L.Zhang**, S.Cosemans, D.J.Wouters, G.Groeseneken, M.Jurczak, "Analysis of the effect of cell parameters on the maximum RRAM array size considering both read and write", *in Proc. ESSDERC*, pp. 282-285, 2012.

Chapter 3: Based on the simulation framework described in Chapter 2, the requirements that a 1S, 1R cell need to fulfill are derived for an array with a reference (fixed) size of 1Mbit, considering constraints corresponding to both read and write operations. By assuming an ideal resistive memory element, the requirements are extracted for both type-I (e.g. generating non-linear I-V characteristics without any abrupt I-V transition) and type-II (e.g. I-V behavior characterized by an abrupt transition) selectors using parameterized characteristics. We find that:

- Besides the non-linearity and the drive current, the operating voltage is another important parameter for type-I selectors, which balances the trade-offs for fulfilling a low voltage operation, large on/off resistance window and high non-linearity 1S1R cell characteristics. Similar performance trade-offs occur for type-II selector, when designing the parameters including threshold voltage and on-state resistance.
- Compared to the type-I device, the advantage of using type-II selector is that it is more favorable to the low operation voltage. However, a challenge remains the limited parameter design margin due to the read disturb issue for the resistive memory to be paired.

Furthermore, we investigated the impact of the on/off resistance ratio of the resistive memory on the 1S1R read performance. Contrary to the conclusions made by other research reports (and becoming a popular "belief"), that a large on/off resistance ratio is always desirable for improving the read margin at array level, we show that:

- For a given selector, an optimal resistance ratio can be determined which gives the best read performance. Pursuing optimization of the resistive memory towards excessively large resistance ratio is not necessary. In fact, it is more effective to improve the read margin by increasing the selector non-linearity, instead of increasing the on/off resistance ratio.

Publications contributing to this chapter:

1. **L.Zhang**, S.Cosemans, D.J.Wouters, G.Groeseneken, M.Jurczak, B.Govoreanu, "On the Optimal On/Off resistance Ratio for Resistive Switching Element in one-selector on resistor (1S1R) Crosspoint array", *IEEE Electron Device Letters*, vol.36, no.6, pp.570-572, 2015.
2. **L.Zhang**, S.Cosemans, D.J.Wouters, G.Groeseneken, M.Jurczak, B.Govoreanu, "Selector design considerations and requirements for 1SIR RRAM crossbar array", *in Proc. International Memory Workshop (IMW)*, pp.34-37, 2014.
3. **L.Zhang**, S.Cosemans, D.J.Wouters, G.Groeseneken, M.Jurczak, B.Govoreanu, "One-selector One-resistor (1S1R) Cross-point Array with Threshold Switching (TS) Selector", *IEEE Transactions on Electron Devices*, vol.62, no.10, pp.3250-3257, 2015.
4. B.Govoreanu, **L.Zhang**, M.Jurczak, "Selectors for High Density Crosspoint Memory Arrays: Design considerations, Device Implementations and Some Challenges Ahead", *in Proc. ICICDT*, invited paper, 2015.

5. B. Govoreanu, A. Ajaykumar, H. Lipowicz, Y.Y Chen, J.C Liu, R. Degraeve, **L.Zhang**, S. Clima, L. Goux, I.P Radu, A. Fantini, N. Raghavan, G.S Kar, W. Kim, A. Redolfi, D.J Wouters, L. Altimime, M. Jurczak, "Performance and Reliability of Ultra-Thin HfO2-Based RRAM (UTO-RRAM)", *in Proc. International Memory Workshop (IMW)*, pp.48-51, 2013.

Chapter 4: A novel Metal/Silicon/Metal (MSM) device using ultra-thin undoped amorphous silicon is proposed for two-terminal RRAM selector applications. The doping-free MSM behaves as a low bandgap insulator and provides bidirectional non-linear characteristics by tunnelling conduction.

- The proposed selector shows a high current drive (>1MA/cm^2), high non-linearity (over hundred), tunable operating voltage range and fast switching speed (<1ns).
- By including annealing and barrier engineering, we show optimized MSM structures with an improved half-bias non-linearity over 6000. Excellent reliability is demonstrated, with statistical ability to withstand bipolar cycling of over 10^5 at drive current condition and thermal stress at $125\,^{\circ}\mathrm{C}$ for 3hours with negligible degradation.
- We identify that the trap generation in the amorphous silicon layer is responsible for the selector degradation during the electrical stress, affecting its non-linearity.
- By combining the proposed selector with a typical HfO_2-based resistive memory ($\pm$1.5/10μA), simulation results suggest that operation of the 1S1R full cell requires around $\pm$5V. It is expected that less than 0.4V voltage drop during the write operation and over 45% of read margin can be achieved for an 1Mbit array.

Publications contributing to this chapter:

1. **L.Zhang**, A.Redolfi, C.Adelmann, S.Clima, I.P.Radu, Y.Y.Chen, D.J.Wouters, G.Groeseneken, M.Jurczak, B.Govoreanu, "Ultrathin Metal Amorphous-Silicon Metal Diode for Bipolar RRAM Selector Applications", *IEEE Electron Device Letters*, vol.35, no.2, pp: 199-201, 2014.
2. **L.Zhang**, B.Govoreanu, A.Redolfi, D.Crotti, H.Hody, V.Paraschiv, S.Cosemans, C. Adelmann, T. Witters, S. Clima, Y. Y. Chen, P. Hendrickx, D. J. Wouters, G. Groeseneken, M.Jurczak,"High-Drive Current (>1MA/cm^2), Highly Nonlinearity (>10^3) TiN/Amorphous Silicon/TiN Scalable Bidirectional Selector with Excellent Reliability and Its Variability Impact on the 1S1R Array Performance", *in Proc. IEDM*, pp.164-167, 2014.
3. B.Govoreanu, **L.Zhang**, D.Crotti, Y.-S.Fan, V.Paraschiv, H.Hody, T.Witters, J.Meersschaut, S.Clima, C.Adelmann, M.Jurczak, "Thin-Silicon Injector (TSI):

an All-Silicon Engineered Barrier, Highly Nonlinear Selector for High Density Resistive RAM Applications", *in Proc. IMW*, pp.1-4, 2015.

4. B.Govoreanu, C.Adelmann, A.Redolfi, **L.Zhang**, S.Clima, M.Jurczak, "High-Performance Metal-Insulator-Metal Tunnel Diode Selectors", *IEEE Electron Device Letters*, vol.35, no.1, pp.63-65, 2014.

Chapter 5: We presented a variability-aware 1S1R array performance assessment methodology. The variability-aware array performance assessment accounts for three independent variability sources: data pattern randomness, selector and on/off resistance variation. By injecting selector variability using the experimental data from our reference MSM selector (detailed in Chapter 4), our analysis points out that:

- The selector is another important array variability contributor and mainly affects the LRS readout current, causing additional read margin degradation. Therefore, to accommodate cell variation and guarantee acceptable read performance, improved cell characteristics are required to enable a robust, variability-aware 1S1R array design.

We further assessed the 1S1R cell requirements for a 1Mbit array including cell variability.

- With a selector variation σ_r=0.2, a minimal on/off resistance ratio of 5 and selector half-bias non-linearity (NL½) of about 8000 are required to obtain 10% of the read margin.

Publications contributing to this chapter:

1. **L.Zhang**, B.Govoreanu, A.Redolfi, D.Crotti, H.Hody, V.Paraschiv, S.Cosemans, C. Adelmann, T. Witters, S. Clima, Y. Y. Chen, P. Hendrickx, D. J. Wouters, G. Groeseneken, M.Jurczak,"High-Drive Current (>1MA/cm^2), Highly Nonlinearity (>10^3) TiN/Amorphous Silicon/TiN Scalable Bidirectional Selector with Excellent Reliability and Its Variability Impact on the 1S1R Array Performance", *in Proc. IEDM*, pp.164-167, 2014.
2. **L.Zhang**, S.Cosemans, D.J.Wouters, G.Groeseneken, M.Jurczak, B.Govoreanu, "Cell Variability Impact on the 1S1R (One-selector One-Resistor) Cross-point Array Performance", *IEEE Transactions on Electron Devices*, Special issue for IEDM 2014, accepted, 2014.

Chapter 6: We extended the cross-point array model (discussed in Chapter 2) by enabling a quantitative analysis on the vertical 3D RRAM structure. Our simulation results suggest that, for vertical RRAM:

- The read margin is more sensitive to the number of layers compared to in plane array size in the matrix.
- Write performance is more sensitive to bias conditions. Optimized bias conditions can be found for improving the write margin and reducing the power consumption.
- Compared to stacked 3D architecture, assuming self-rectifying cells (SRC) with moderate non-linearity, Vertical RRAM is more promising for both read and write operations.

Publications contributing to this chapter:

1. **L.Zhang**, S.Cosemans, D.J.Wouters, B.Govoreanu, G.Groeseneken, M.Jurczak, "Analysis of Vertical Cross-Point Resistive Memory (VRRAM) for 3D RRAM Design", *in Proc. IMW*, pp.155-158, 2013.

7.2.2 Timeline

This Ph.D. titled "Study of the selector element for resistive memory" started in the fall of 2011. It is supported by the emerging memory program for RRAM at imec, Leuven, Belgium and the electrical engineering department (ESAT) of KULeuven, Belgium.

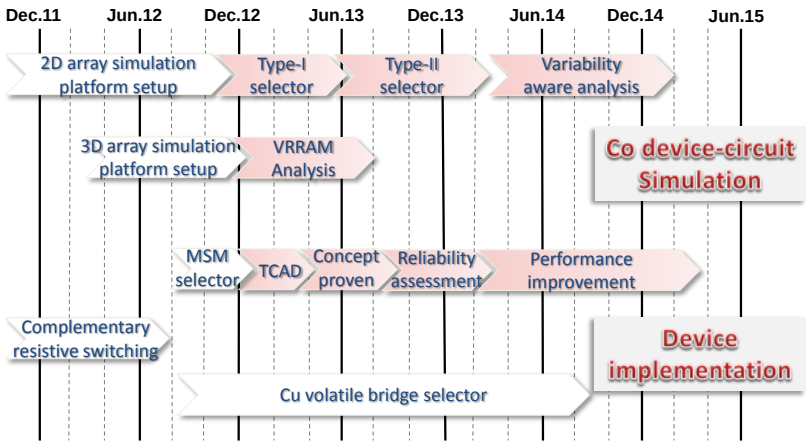


Figure 7.1: *Timeline of the Ph.D. work.*

Fig.7.1 summarizes the timelines for this Ph.D.. Based on the simulation platform developed at the beginning of the research work, different areas of focus were considered through the past four years, focusing on the circuit-device interaction simulation analysis on the 2D 1S1R cross-point arrays.

Next to it, different selector concepts such as MSM, complementary resistive switching (selectorless cell), Cu-based volatile bridge selectors, etc were evaluated experimentally. Among them, the MSM selectors show the most promising characteristics, thus received more emphasis. Fig.7.2 depicts the 300mm wafers turns measured during the Ph.D., indicating the two stages of experimental work, namely the initial selector proof of concept stage, and the device optimization stage.

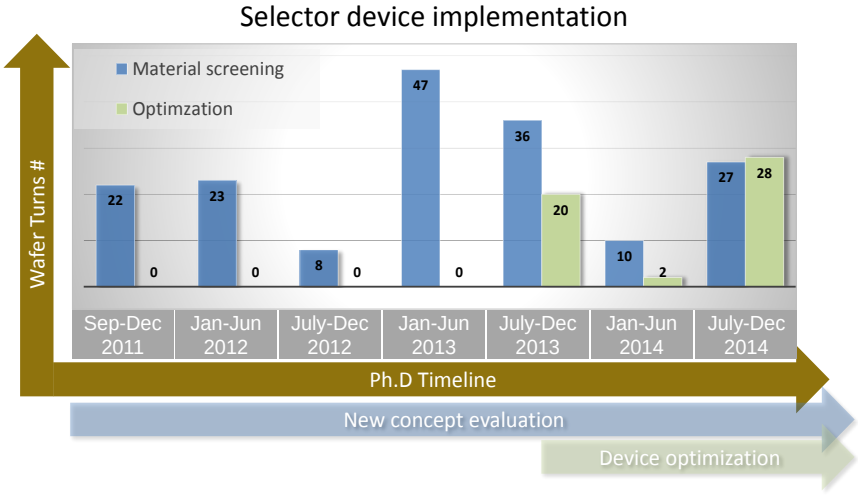


Figure 7.2: *Wafer turns through the Ph.D.*

7.3 Outlook and future work

7.3.1 Future work

Implementation of stacked 1S1R devices is a very tough task, therefore, at the initial stage of this Ph.D., we predicted the impact of 1S and 1R device parameters on the array performance using a simulation approach, to provide engineering guidance for device implementation. Concerning the future work related to the 1S1R simulation, two aspects deserve further exploration including:

- Confirm the accuracy of the synthesized 1S1R I-V characteristics.

Currently, the 1S and 1R devices are developed individually. The full cell characteristics are predicted by simply synthesizing the I-Vs from the two individual elements. It is important to compare the aggregate characteristics of a full stacked 1S1R cell (need to be developed) against the series combination of the same 1S and 1R, in order to confirm the accuracy of the simulation prediction.

- Improve the circuit model for enabling AC transient analysis.

The circuit model developed in this Ph.D. only enables DC analysis. However, DC operations are not practical in real memory circuits. For providing more accurate analysis results, AC transient simulations are necessary. This requires sophisticated analytical models for both resistive switching memory and selector to be developed. Moreover, the parasitic resistance and capacitance (RC) become more important when AC analysis is involved. This may require RC extraction from the real drawn layout of cross-point arrays, instead of assuming simple R, C values in the circuit schematic.

- Periphery circuits design for cross-point arrays.

When 'qualified' resistive memory and selector have been developed, the next step is the periphery circuits design. This study would provide deep insight on the practical behavior of resistive memory arrays. Based on this, the additional performance indicators such as read/write access time and energy consumption can be evaluated in the FOM analysis. These parameters are very important for assessing the possibility of using RRAM, either as replacement for the existing NVM technologies or acting as Storage Class Memory to improve the current memory hierarchy. Moreover, RRAM cross-point arrays could be also interesting for neuromorphic applications or logic-in memory computing. In that case, the feasibility of multi-bit array operation needs to be analyzed in advance.

Concerning selector device implementation, for our best performed MSM and TSI selectors, the foremost thing is to further improve their drive current. This can be possibly achieved, by

- Further scaling of the devices down to 10nm-size.
- Replacement of the TiN electrode with lower workfunction metals.

At last, as suggested by the simulation (Chapter 3), the threshold switching selector is more favorable for the low voltage operation as compared to the type-I selectors. It seems that the threshold switching is worthy of attention in the future.

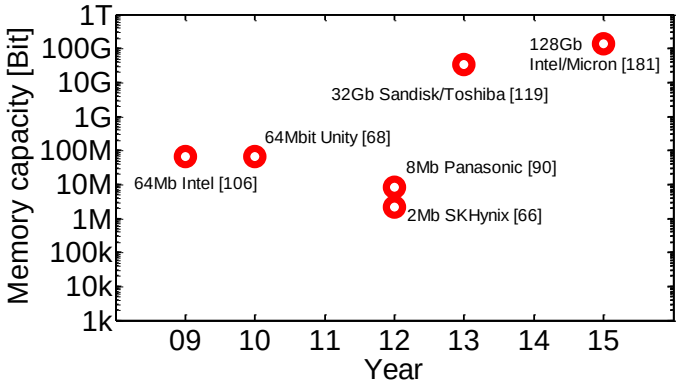


Figure 7.3: *Reported cross-point memory capacity [66, 68, 90, 106, 119, 181].*

7.3.2 RRAM technology outlook

The concept of resistive memory has been proposed for more than 40 years, recently, it received more and more attention and is considered as the most promising candidate among other emerging non-volatile memory technologies for the future mass data storage application, e.g. NAND Flash replacement. Unfortunately, several shortcomings of RRAM technologies have been realized during recent research. Nowadays, with the successful production of 3D NAND Flash and its continuous development, whether or not RRAM will become a successor of NAND remains questionable.

However, god is fair to anyone (any technology). When he closes one of your doors (market), he will open another for you. (i) the embedded NOR Flash is facing its physical limitations where RRAM technology may become a big hope to tap into the market for sub-40/28nm technology node; (ii) the emerging Internet-of-Things (IoT) needs ultra-low power memories where RRAM can fit in; (iii) the new type storage class memory (SCM), changing the current memory hierarchy in computer systems, also offer RRAM an opportunity.

Nevertheless, the most interesting application for RRAM remains high density memory which can offer gigabytes or even larger capacity at low costs. This requires devices to be densely packed in memory arrays, operating without wasteful parasitic leakages. Therefore, the development of selector device technologies for cross-point arrays, will be rather important for the mass production for RRAM. Indeed, the recent progress of the cross-point array development (Fig.7.3) shows a warming sign!

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Scientific publications

Invited journal paper

1. **L.Zhang**, S.Cosemans, D.J.Wouters, G.Groeseneken, M.Jurczak, B.Govoreanu, "Cell Variability Impact on the 1S1R (One-selector One-Resistor) Cross-point Array Performance", *IEEE Transactions on Electron Devices*, Special issue for IEDM 2014, accepted, 2015.

Journal contributions

1. **L.Zhang**, S.Cosemans, D.J.Wouters, G.Groeseneken, M.Jurczak, B.Govoreanu, "One-selector One-resistor (1S1R) Cross-point Array with Threshold Switching (TS) Selector", *IEEE Transactions on Electron Devices*, vol.62, no.10, pp. 3250-3257, 2015.

2. **L.Zhang**, S.Cosemans, D.J.Wouters, G.Groeseneken, M.Jurczak, B.Govoreanu, "On the Optimal On/Off resistance Ratio for Resistive Switching Element in one-selector on resistor (1S1R) Crosspoint array", *IEEE Electron Device Letters*, vol.36, no.6, pp.570-572, 2015.

3. **L.Zhang**, A.Redolfi, C.Adelmann, S.Clima, I.P.Radu, Y.Y.Chen, D.J.Wouters, G.Groeseneken, M.Jurczak, B.Govoreanu, "Ultrathin Metal Amorphous-Silicon Metal Diode for Bipolar RRAM Selector Applications", *IEEE Electron Device Letters*, vol.35, no.2, pp. 199-201, 2014.

4. Y-S.Fan, **L.Zhang**, D.Crotti, T.Witters, M.Jurczak, B.Govoreanu, "Direct Evidence of the Overshoot Suppression in Ta_2O_5-Based Resistive Switching Memory with an Integrated Access Resistor", *IEEE Electron Device Letters*, accepted, 2015.

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10. D.J.Wouters, **L.Zhang**, A.Fantini, R.Degraeve, L.Goux, Y.Y.Chen, B.Govoreanu, G.S.Kar, G.Groeseneken, M.Jurczak, "Analysis of Complementary RRAM Switching", *IEEE Electron Device Letters*, vol.33, no.8, pp.1186-1188, 2012.

Conference contributions

1. **L.Zhang**, B.Govoreanu, A.Redolfi, D.Crotti, H.Hody, V.Paraschiv, S.Cosemans, C. Adelmann, T. Witters, S. Clima, Y. Y. Chen, P. Hendrickx, D. J. Wouters, G. Groeseneken, M.Jurczak,"High-Drive Current (>1MA/cm^2), Highly Nonlinearity (>10^3) TiN/Amorphous Silicon/TiN Scalable Bidirectional Selector with Excellent Reliability and Its Variability Impact on the 1S1R Array Performance", *in Proc. IEDM*, pp.164-167, 2014 (with presentation).

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Curriculum Vitae

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